SLT DESIGNER'S HANDBOOK
(30-Nanosecond Family)

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1.1 SCOPE. The attached document is intended for use as a guide for machine designers becoming involved in SLT Technology.

1.2 OBJECTIVE. To present a minimum, yet adequate, amount of information for SLT orientation.

1.3 APPLICABILITY. This bulletin applies to IBM machines using SLT Technology (specifically treats with 30-nsec family).

1.4 SOURCE. Information was originated by D. C. Brugnolotti, Dept. 687, Communications Product Engineering, SDD - Kingston, N. Y. as a result of a program originated in Dept. 514, Goddard Real Time Engineering, SDD - Kingston, N. Y.

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SLT Designer's Handbook (30-Nanosecond Family)

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INTRODUCTION

This manual was initially written to aid in the design of a specific machine and was intended as a tool for the logic designer. It is not intended to be all-limiting or inclusive, but as an aid in the application of a logic family. Although this manual covers the 30 nanosecond family, several 5 and 700 nanosecond references are made for clarity.

Contained herein is a list of logic card part numbers considered to be basic building blocks, along with ground rules for their application. The circuit schematics and logic diagrams are listed numerically according to part numbers in the Reference Section of this manual following the text. When both the circuit schematic and logic diagram are available, the schematic follows the logic diagram.

> NOTE: Check the latest machine runs of the CALM list to determine the validity of part numbers.

Also included in this manual are the following:

- List of Condensed Circuit Specifications for applicable circuit modules.
- Schematic diagrams of all SLT circuit modules.
- Information necessary for the application of the basic circuit, i.e., input load constants, output current available (drive equations), power dissipation, power supply requirements, etc.
- General information, i.e., distributed capacity, passive delays, wire resistance, etc.

ABBREVIATIONS (For SLT)

A	AND
A	AND Circuit
A	AND Invert
A-2, A-3	Threshold
ACT	AC Trigger
AI	AND Invert
AIT	AND Invert Terminate
ALD	Automatic Logic Diagram
AOI	AND OR Invert
AOPI	AND OR Power Invert
AOPX	AND OR Power Extend
AOX	AND OR Extend
API	AND Power Invert
AR	Amplifier
Array	Array
C	Capacitor
Cap	Capacitor
Cabl	Cable
CD	Core Driver
Chan	Channel
Cl	Cell
Clk	Clock
Cntl	Control
Cntr	Counter
CR	Diode
CS	Current Switch
Ctl	Control
Ctr	Counter
CV	Converter
D	Driver
DCI	Direct Coupled Invert
DL	Delay Line
DLD	Delay Line Driver
Dly	Delay
Dvr	Driver
Entr	Entrance from Machine Type
Even	Even Count
Excl	Exclusive
Exit	Exit to Machine Type
FDD	Four Dual Diodes
FF	Flip Flop
FFL	Flip Flop Latch
FL	Flip Flop Latch or Flip Latch
FTZ	Four Transistors
Fuse	Fuse
HD	Magnetic Head Driver
HP	High Power
HPD	High Power Driver
HS	High Speed
I	Invert
Inv	Invert
ICN	Indicator Coupling Network
ID	Indicator Driver
IDL	Indicator Driver Lamp
II	Isolating Inverter
Ind	Indicator
Ja	Jack
Jack	Jack
Jmpr	Jumper
L	Inductor
Ld	Loaded
Ld	Transmission Line Driver
Lim	Limiter
Lmp	Lamp
Lp	Loop
LS	Low Speed
LSA	Line Sensing Amplifier
LT	Transmission Line Terminate
LTN	Line Terminating Network
Mach	Machine
MD	Magnet Driver
Mem	Memory
Mltplx	Multiplex
MS	Medium Speed
N	Invert
NL	No Load
Odd	Odd Count
OE	Exclusive OR
OI	OR Invert
OIT	OR Invert Terminate
OR	OR
OR	OR Circuit
OR	OR Invert
Osc	Oscillator
PB	Push Button
PH	Polarity Hold
Plgbl	Pluggable
Pwr	Power
Pwr	Power Supply
R	Resistor
Res	Resistor
RC	Resistor-Capacitor
Rcvr	Receiver
Rd	Read, Reed
Reg	Register
Rly	Relay
RW	Read-Write
Sel	Select
Ser	Serial
Serv	Service
Serv	Service-Voltage
SLT	Solid Logic Technology
SPD	Sample Pulse Driver
Spec	Special
SS	Singleshot
SSL	Singleshot Low Speed
SSA	Singleshot Medium Speed
ST	Schmitt Trigger
SW	Switch
T	Terminate
TD	Time Delay
Tgr	Trigger
Ther	Thermal Switch
Ther	Thermal Switch
TLR	Transmission Line Resistor
TLT	Transmission Line Terminate
Tx	Transistor
V	Voltage Amplifier
Var	Variable
X	Extend
XOI	Exclusive OR Invert
XOR	Exclusive OR
XORL	Exclusive OR Latch
Xtl	Crystal
Z	Impedance

GLOSSARY

Basic refers to the standard design of the machine; it includes optional features (MFI's) if drawn as part of the standard logic page. "Basic" is in contrast to "Version."

Circuit Number consists of five alphameric characters of the form ANNAA, which uniquely define a particular basic circuit.

Design Automation refers to the programs that prepare and print the ALD's. They consist of four major stages of processing: Logic Master Tape, Simulation, Packaging and Checking, and Physical Master Tape. The outputs consist of documents to aid engineering in the development of computers, release documents (ALD's), and tapes for manufacturing.

DOT-Block is an ALD block used on ALD logic pages to show "DOT-AND" and "DOT-OR" functions, which are physically accomplished by tying two signals together at a pin. Thus, one logical net on the ALD is combined with other logical nets by the DOT-block to produce one combined physical net.

NOTE: One DOT-block does not connect to another DOT-block.

Grouping refers to the associating of certain circuit configurations prior to partitioning. Circuits represented on the ALD's by more than one block but always found on the same card are said to be in the same group.

Logic Master Tape (LMT) is the machine language record in logic page order. Each time a portion of this machine record is altered, logic pages containing the changes are produced for the engineer.

Net is a complex of nodes, normally pins or connectors on the ALD, all common electrically.

Net Number consists of the source block page number, block serial number, and output line position of the source block. It consists of eight alphameric characters of the form AANNNAAB (A-alphabetic, N-numeric, B-either alphabetic or numeric).

Node is one circuit end point of a net (such as a pin on a card or a connector on a board).

Packaging and Checking refers to a series of programs that aid the engineer in the physical packaging of the logic and check data that is manually inserted on the pages.

Partitioning refers to that part of the design automation program that breaks up logic into cards and assigns the cards to boards.

Physical Master Tape (PMT) is a machine language record of the physical aspects of the design. It is arranged in physical sequence. Its purpose is (1) to retain in a convenient form the physical data from LMT, as well as the physical data from the PMT (wiring data primarily), (2) to retain the physical design at a fixed level while the logical design is undergoing change, and (3) to extract information from the tapes at the request of the engineer or other users.

Pins are the male parts of the connection between card and board or between cable connector and board.

Portion refers to those circuits on a card that are connected together by printed wiring.

Signal Name is the title, may be blank, that gives meaning to a logical net; each net has only one signal name.

Simulation refers to programs that allow the engineer to dynamically exercise the logic before the machine is packaged.

Sink is the end or ends of a net to which signals flow.

Source is the beginning of a net from which signals flow.

Symbolic Package is two characters to be used by design automation in the partitioning and placement programs. Blocks with the same characters in the symbolic package field are placed on the same board by the card partitioning program.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

Version is a term used by design automation and indicates the particular manner in which logic records are kept for certain features; a feature is a version of its records and is kept as an add-delete (by block) to the basic records.

NOTE: "Version" gives automatic or implied updating of the feature by the basic, since an added basic block is in effect in the version.

Version Page is the ALD page made up of all blocks on the basic page which appear unchanged in the version design, plus additional version blocks needed to change the basic page into the version page.

Via Hole is the plated-through hole which may or may not contain a pin; it is used exclusively as a contact between conducting layers of the board. It is not considered a node.

SLT COMPONENT CIRCUITS

GENERAL

- Solid Logic Technology (SLT) is the technology of current IBM systems.
- Chip, module, card, board, and gate are the physical building blocks.
- Circuit speeds demand computer use for figuring wire lengths.

SLT (Solid Logic Technology) is the new technology applicable to current IBM products. Microminiaturization techniques are used in the production of devices for high-speed computers.

The basic semiconductors are the dual diode and the transistor chip. These chips are about the size of a grain of salt. The chips, along with screened resistors and interconnections, are packaged in 1/2 inch square modules. The modules may have 12 or 16 pins for connections to the card.

The module and other electronic components are designed into circuits that have three operating speeds: 700 nanoseconds (slow speed), 30 nanoseconds (medium speed), and 5-10 nanoseconds (high speed).

The modules and other electronic components are mounted on cards. The card plugs into an 8-1/2 x 12-1/2 inch board. The boards are cabled into gates. The gates are cabled together to form the machine or system.

Design automation has developed several programs for SLT. One of these programs, called ALD's (Automated Logic Diagrams), is the computer-generated logic of the machine or system. Another computer program designs the printed wiring of the boards for optimum operation.

As machines operate at faster speeds, wire lengths between components become a design problem. Electricity travels at about 186,300 miles a second, which equals 11.8 inches a nanosecond. Assuming one nanosecond of delay for approximately each foot (11.8 inches) of wiring, the wiring paths for circuits in the 5-10 nanosecond range of operation can become critical. The design automation program calculates wiring paths on the card and board so that wire lengths and circuit paths are a minimum distance.

PHYSICAL DESCRIPTION

The smallest physical component is the dual diode or transistor chip, which is 0.025 inch square. The chip is mounted on the substrate along with other chips, screened resistors, and the printed wiring. The substrate and its components are encapsulated to form a module. The module is about 1/2 inch square. Modules and molded R-C components are mounted on pluggable cards. The cards

have a printed land (wiring) pattern and, generally, a voltage-ground plane. Card sizes are such that 6, 12, 24, or 30 modules may be mounted on each card. The cards may plug into one or two sockets depending upon the particular type of card. (Figures 1 through 4.)

The cards plug into an SLT board. The board has a printed land (wiring) pattern on both sides, a voltage plane, and a ground plane. The physical size of the board is 8-1/2 inches wide and 12-1/2 inches high. Boards are mounted on gates and interconnected by flat cables. The gates are interconnected and make up a machine or box.

In summary, physical size from the smallest to the largest is: chip to module to card to board to gate to frame to machine.

PHYSICAL DESIGN OF CIRCUITS

The physical building blocks of SLT are the module, card, board, and gate. The physical building blocks of the electronic circuit (the function block as found on the ALD page), are the modules and the printed land pattern of the card. The modules are designed so that they may be used separately or in combination with other modules or separate components. Circuits are designed to use parts of modules in combination with other modules or parts of modules and/or components. For example, Figure 48 shows that the medium speed singleshot consists of: one-half of an FDD, R-1 of an R-pack, one-half of an I I module, one-half of a DCI module, a timing capacitor, and all the separate parts connected by the printed land pattern of the card.

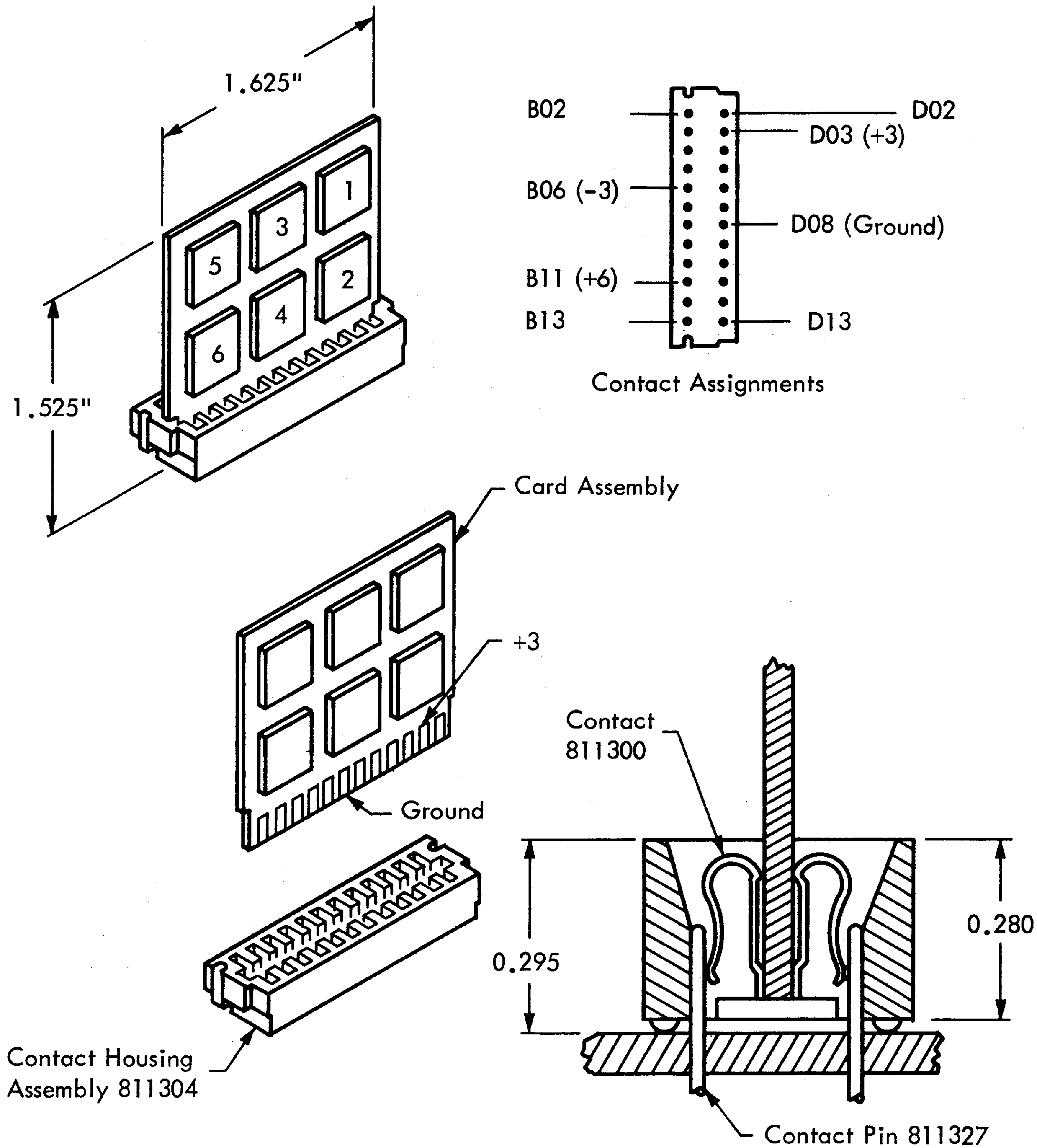


Figure 1. 1 - 6 PAC

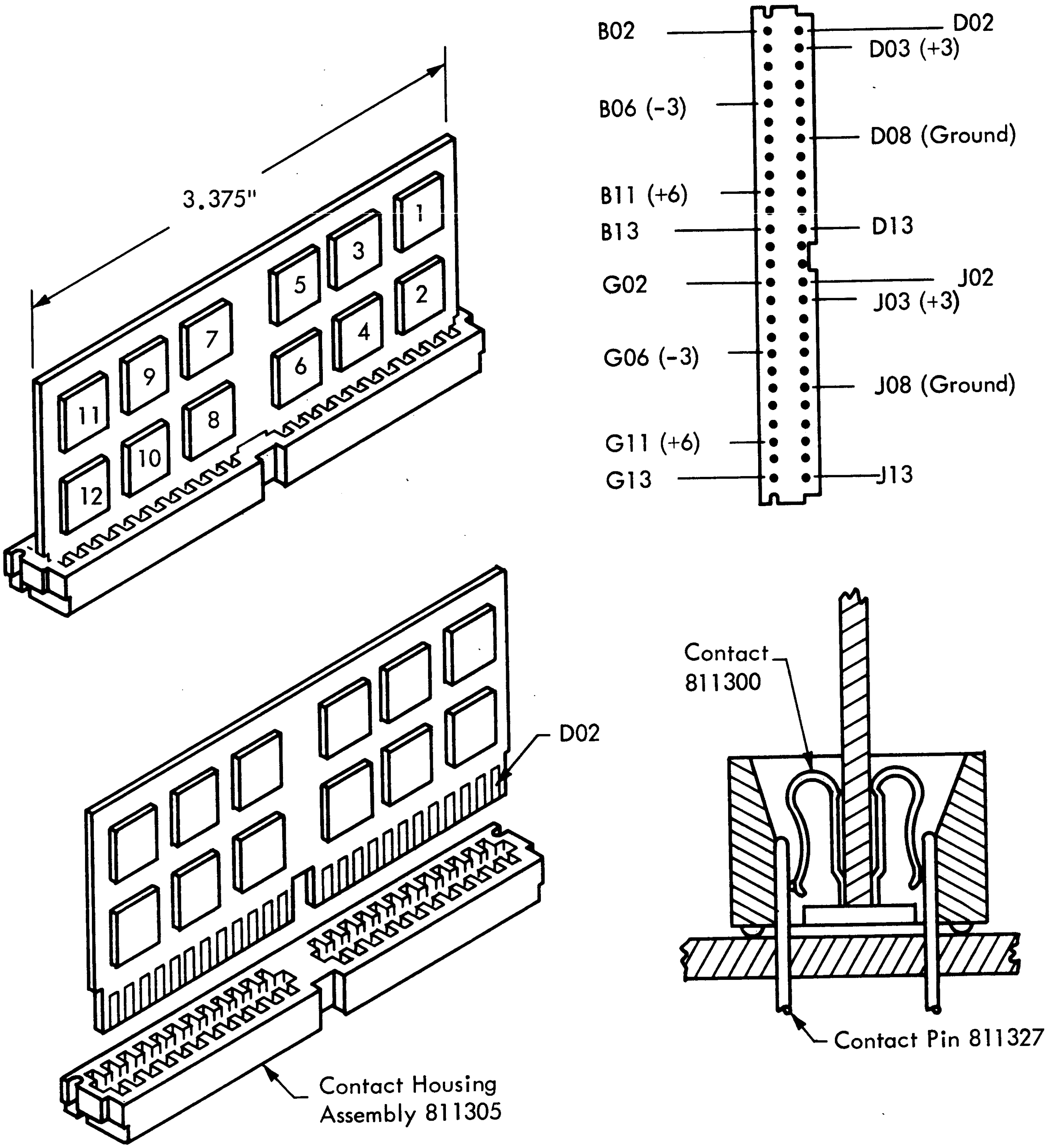


Figure 2. 2 - 12 PAC

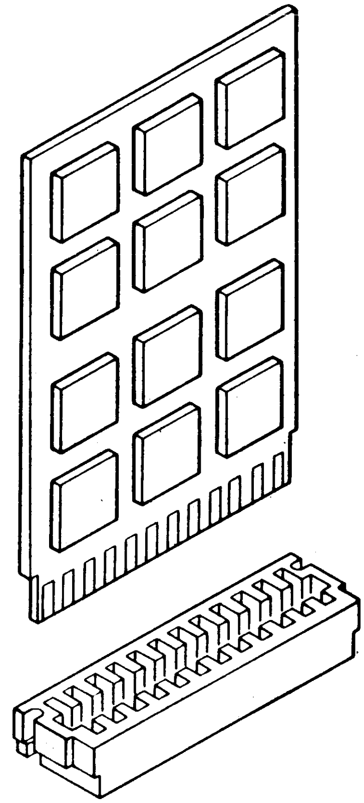


Figure 3. 1 - 12 PAC

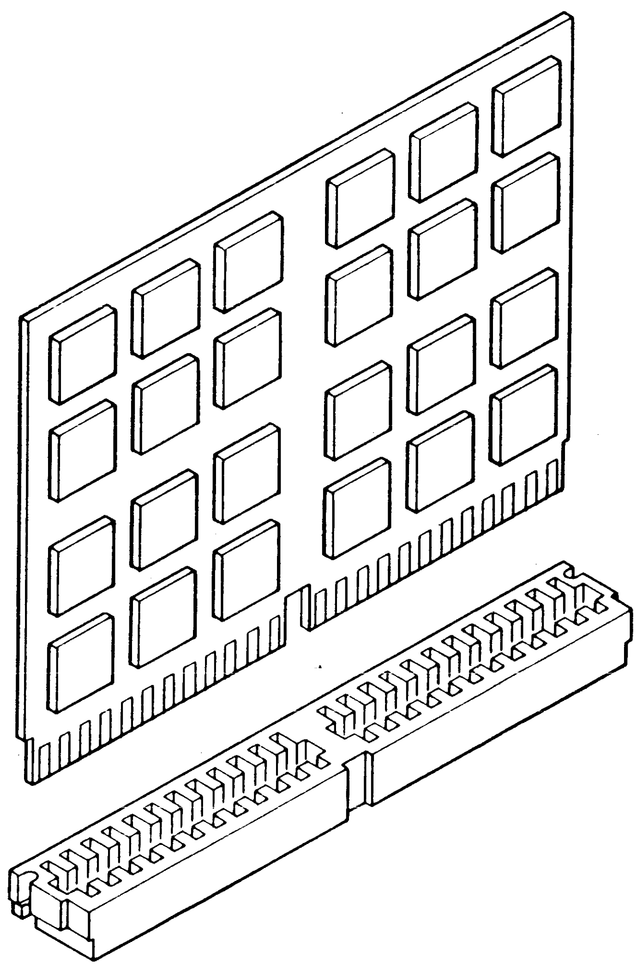


Figure 4. 2 - 24 PAC

SLT CIRCUITS

- The basic SLT circuit is the AND - OR - Invert (AOI).
- Circuit Speeds are: 5-10 nsec, 30 nsec, and 700 nsec.
- Voltage levels are: 0.9 to +3.0v, +0.0 to +3.0v, 0.0 to +12.0v, respectively.
- Logic may be diode, transistor, or a combination.
- A logic block may use different circuits for each of the three speeds.

A transistor circuit can be approached and understood in terms of knowing the logic relation of the inputs to the outputs, or knowing the power dissipation of components and the relation of loading and input transition times to circuit delays.

Circuit information is restricted to:

1. Relation of circuit inputs to circuit outputs.
2. How the circuit converts input signals to output signals.
3. Important input and output requirements.

The manual describes only those SLT circuits that are most widely used.

CIRCUIT SPEEDS

Presently there are three circuit speeds. The circuit speed is dependent upon the semiconductor used. The circuit speeds are in the order of 10, 30, and 700 nanoseconds for each logical block.

CIRCUIT VOLTAGES

Approximate voltage levels for each of the three circuit speeds are:

5-10 nsec circuit:	+0.9v, most negative; +3.0v, most positive.
30 nsec circuit:	+0.0v, most negative; +3.0v, most positive.
700 nsec circuit:	+0.0v, most negative; +12.0v, most positive.

TRANSITIONS

Transition (Figure 5A) is the time a transistor takes to switch. The transition points for the different families are:

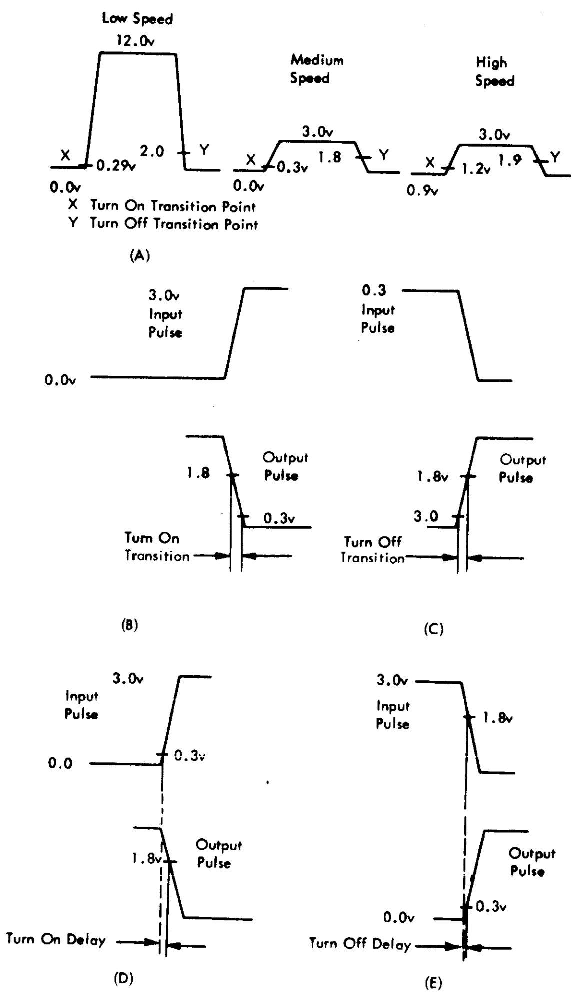


Figure 5. Transitions and Circuit Measurements

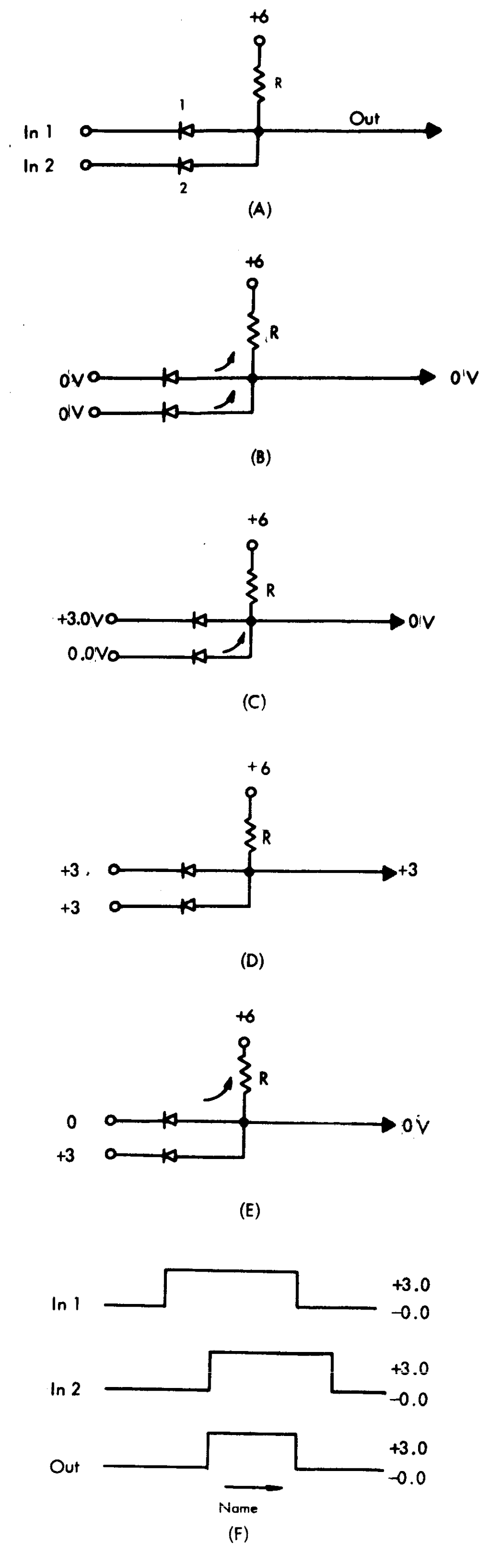


Figure 6. The AND Gate

Family	Transition Points
5-10 nsec high speed	+1.2v, 1.9v
30 nsec medium speed	+0.3v, 1.8v
700 nsec low speed	+0.29, 2.0v

The different transition times are turn-on-transition, turn-on delay, turn-off transition, and turn-off delay. These values are basically the same for each of the circuit families. The major difference is that the transition points and voltage levels vary for each family.

Turn-on transition (Figure 5B) is the switching time from an off state to an on state. Turn-on transition is measured on the output waveform from a specified value in the nonconducting state to a specified value in the conducting state.

Turn-off transition (Figure 5C) is the switching time from an on state to an off state. Turn-off transition is measured on the output waveform from a specified value in the conducting state to a specified value in the nonconducting state.

Turn-on delay (Figure 5D) is the switching time from an off state to an on state. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

Turn-off delay (Figure 5E) is the switching time from an on state to an off state. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

BASIC CIRCUITS

The basic circuit of SLT is the "AOI" (AND-OR-Invert) (Figures 10, 11 and 19). The AOI comprises an AND gate, an OR circuit, and an inverter. These three circuits are used extensively throughout the computer.

The Diode AND Gate

The AND Gate is a diode AND circuit (Figure 6A). The AND circuit may be considered a plus AND, or a minus OR. The logical operation of these circuits requires:

+AND circuit:	must have all plus inputs for a plus output.
-OR circuit:	has a minus output if either input is minus.

The two circuits are identical; only the logical usage is different. The +AND circuit insures that both inputs are up before the output comes up; the -OR circuit has a minus output as long as any input is down. In this simplified description, the example specifies two diodes. The same description, however, applies to (n) diodes. If both inputs are minus, the polarities are correct for both diodes to conduct (Figure 6B). Because of the low forward resistance of the diodes, the output voltage will be approximately equal to the input voltage.

If input 1 changes instantaneously to a positive voltage, diode 1 is cut off because the cathode is more positive than the plate (Figure 6C). Diode 2, with 0v on its cathode, maintains conduction and the output voltage remains unchanged (0v).

When input 2 also changes to a positive voltage, diode 2 is cut off (Figure 6D). When output voltage reaches +3.0 volts, the diodes go back into conduction. The output remains at +3.0v. When input 1 falls to 0v, diode 1 conducts more heavily, and diode 2 is cut off (Figure 6E). The output follows input 1 down to 0v.

The following truth table applies to Figures 6A through 6E.

	IN		OUT
	1	2	
6B	0	0	0
6C	+3	0	0
6D	+3	+3	+3
6E	0	+3	0

This shows the AND function is satisfied at the +3v level.

The action of an AND circuit (Figure 6F) may be summarized as follows: The output voltage of a plus AND circuit approximately equals the most negative input voltage. This statement applies regardless of the number of inputs.

The Diode OR Circuit

Circuit configurations (Figure 7A) for the +OR and the -AND circuits are identical. Logical operation of these two circuits is as follows:

+OR circuit:	gives a plus output, if an input is plus.
-AND circuit:	requires all minus inputs for a minus output.

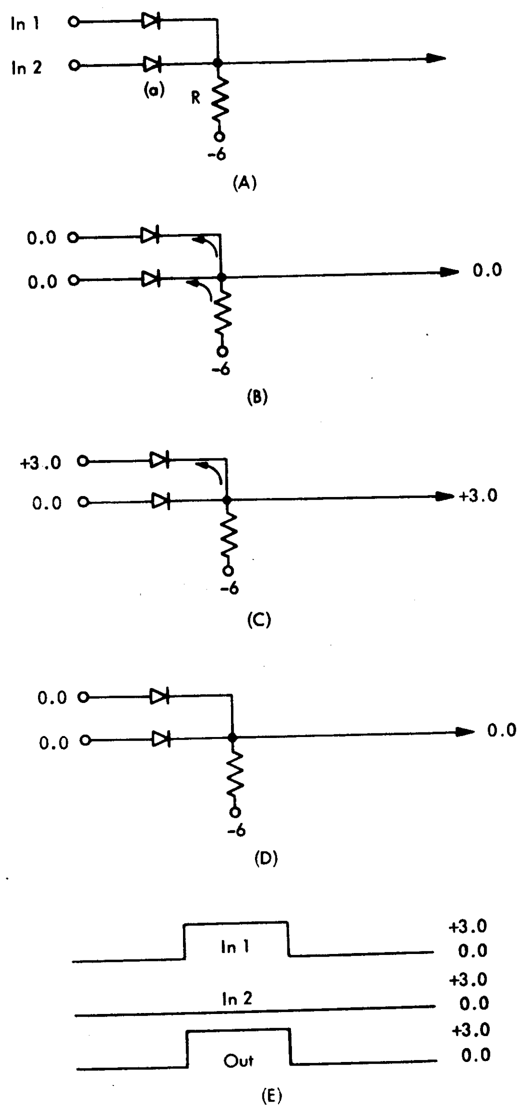


Figure 7. The OR Circuit

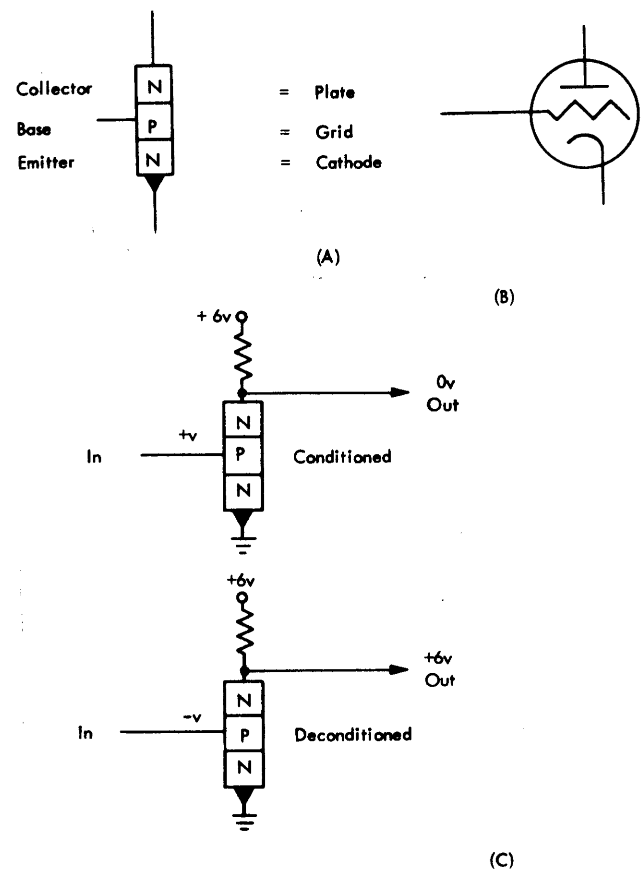


Figure 8. The Inverter

Therefore, the +OR circuit differs from the +AND circuit because the OR circuit needs only one input up to bring the output up.

(In this simplified description, the example specifies two diodes but the description applies as well to (n) diodes.) The operation is as follows: If both inputs are at the most negative level, the polarities are correct for both diodes to conduct (Figure 7B). Thus, the input level determines the output level.

If either input diode rises to the most positive level, that diode conducts more heavily (Figure 7C). The other diode then cuts off and the output follows the input, rising to the most positive level of input voltage. Normally only one input to an OR circuit comes up at a time.

When the input that was up drops, the input diode is cut off (Figure 7D). The input diode conducts again when the output voltage reaches a point slightly more positive than the most negative input level.

The action of a plus OR circuit (Figure 7E) is summarized as follows: The output voltage of a plus OR circuit approximately equals the most positive input voltage.

The Inverter

In SLT circuits, the transistor provides inversion. The inverter used in SLT applications is the grounded emitter transistor of the NPN (P base) type.

The voltages applied to the elements of a transistor are the basis for controlling the transistor's conduction. Figure 8A relates the elements of the transistor and the tube. Transistor conduction, as defined here, is current which flows through the collector or emitter circuit.

Bias is the term given to the control potential in both transistor and tube applications. Bias voltage is the dc voltage difference in potential between the base (grid) and the emitter (cathode). Bias voltage is the controlling factor in transistor conduction.

To determine conduction control, consider the emitter voltage to be held at a constant ground level, then apply the input voltage to the base (Figures 8B, C).

To control the conduction of the transistor, the base voltage must be capable of a level either above or below the emitter voltage.

The following rules cover conduction:

1. An NPN (P base) transistor will conduct if its base is more positive than its emitter.
2. A PNP (N base) transistor will conduct if its base is more negative than its emitter.

In tube theory, if the dynamic resistance between the cathode and plate is decreased by the grid voltage, current will flow in the plate circuit. This theory is also true in transistors; the bias potential changes the dynamic resistance between the emitter and collector, thereby controlling current flow through the transistor. A high dynamic resistance of the transistor results in little or no current flow. The direction of bias potential is called either "forward bias" (which causes conduction) or "reverse bias" (which cuts off conduction).

The property of displaying a large or a small dynamic resistance is the primary consideration in analyzing basic transistor circuits. The resistance parameter is also true in tube theory.

The following rules cover resistance:

1. A conducting (or "conditioned") transistor presents a small resistance to current flow.
2. A cut-off (or "deconditioned") transistor presents a large resistance to current flow.

Even though direction of current flow through a transistor is relatively unimportant in analyzing a circuit, two points should be remembered: (1) Current flows from emitter to collector in an NPN transistor; and (2) Current flows from collector to emitter in a PNP transistor. Remember also that even though current will flow against the direction of the arrowhead indicating the emitter (Figure 8C), current will always flow from negative to positive, so that:

1. The collector of an NPN must be returned to a more positive voltage than its emitter.
2. The collector of a PNP must be returned to a more negative voltage than its emitter.

Operating Characteristics. A conducting diode must have ground (0.6v) on the anode and +0.0v on the cathode. There is approximately a 0.6v drop across a conducting diode.

A transistor with a grounded emitter will be cut off with 0.3v at the base. An input voltage above 0.3v will start a transistor into conduction. With 0.8v at the base, the transistor will conduct to saturation.

The translate diode (Figures 10 & 11, Diode 5, i.e., the diode between the AND gate and the transistor acting as an OR diode) suppresses noise and provides uniform voltage at the base of the transistor. The voltages are 0.3v for cutoff and 0.8v for saturation.

CIRCUIT DESCRIPTIONS

The AND-OR-Invert circuit is used in many ways; the more common usages are included here.

Note that there are differences in the medium and high-speed AOI circuits; i.e., the AOI, medium speed (Figure 11), and the AOI_{10}, high speed (Figure 19).

AND Invert (AI)

The AI (Figure 9) consists of a diode positive AND circuit followed by a saturating transistor inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 is available for extending the fan-in to the AND by connecting it to common anode diodes from an FDD or AOX module. Pins 8 and 9 are connected on the card for most applications. However, when collectors are dotted, only one collector resistor is needed for the common collector connection. If more collector resistors are connected, the fan-out is reduced accordingly.

The output, pin 9, fans out to a maximum of 5 AI loads for medium speed circuits, and to a maximum of 7 AI/AOI loads for slow speed circuits.

AND-OR Invert (AOI)

The AOI module (Figures 10 & 11) consists of a three-way diode positive AND function and one diode for an OR function, followed by a saturating transistor inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 will extend the fan-in to the AND by connecting it to the common anode diodes of the FDD module. Pin 1 can extend the OR fan-in from the OR diode of the AOX (or AOX_2) module. The maximum OR fan-in is 5.

The output pins, 8 and 9, are connected on the card for most applications. However, when collectors are dotted, only one collector resistor may be connected to retain the specified fan-out capability. The AOI can drive a maximum of 5 AOI circuits (low speed) or 7 AI/AOI circuits (medium speed).

AND-OR Extend (AOX)

The AOX module (Figures 12 through 16) has two identical extender circuits on one substrate. The extender circuits are used with the AI, AOI, API, and ACT to increase the input capabilities of these circuits. Each extender circuit can:

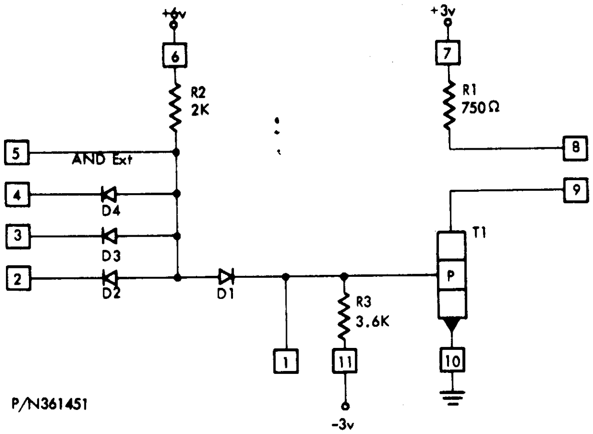


Figure 9. AND-Invert, Medium-Speed (AI)

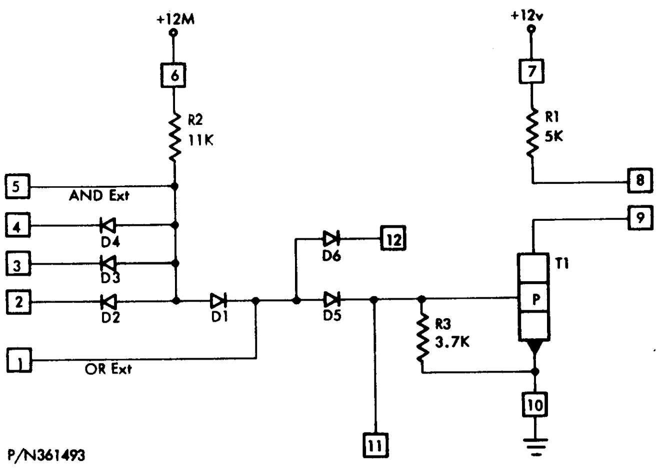


Figure 10. AND-OR-Invert, Low-Speed (AOI)

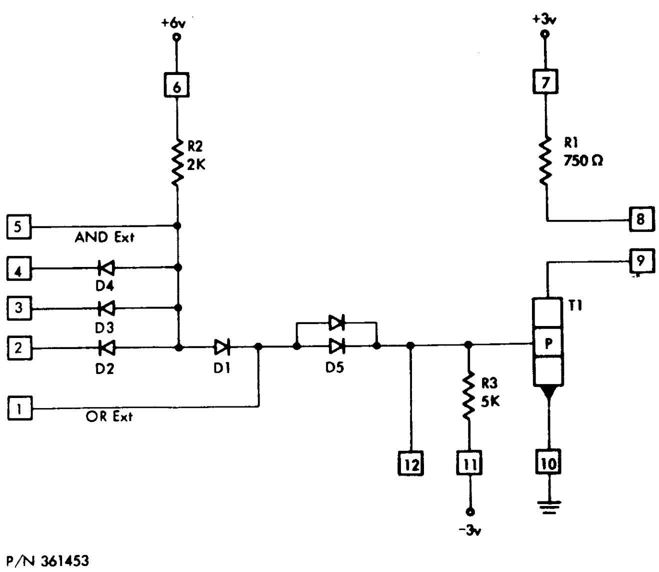


Figure 11. AND-OR-Invert, Medium-Speed (AOI)

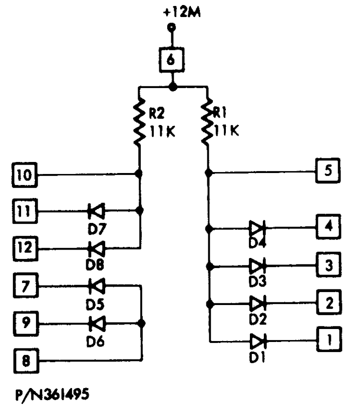


Figure 12. AND-OR-Extend, Low-Speed (AOX₁)

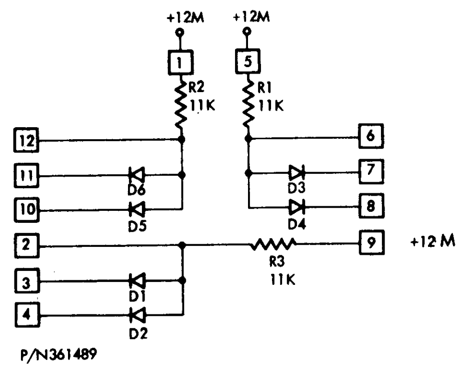


Figure 13. AND-OR-Extend, Low-Speed (AOX₂)

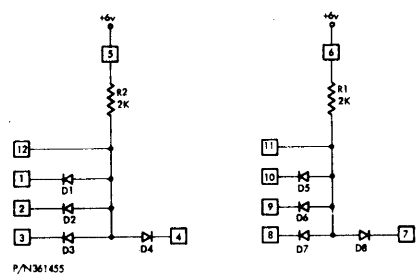


Figure 14. AND-OR-Extend, Medium-Speed (AOX)

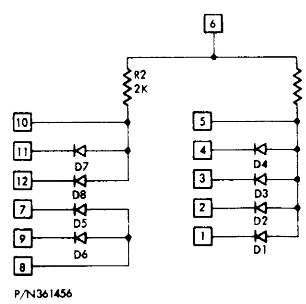


Figure 15. AND-OR-Extend, Medium-Speed (AOX₃)

1. Increase the AND fan-in of the AI and AOI by four.
2. Increase the OR fan-in of the AOI by one while simultaneously increasing the AND fan-in by three.
3. Increase the number of AC gates on one side of one ACT by three.
4. Provide one DC set input for the ACT.
5. Increase the AND fan-in of the API by four; this requires two extender circuits.

AND Power Inverter (API)

The API module (Figure 17) is used as a power inverter with input logic capability. The API serves the same logic function as the AI module, and can drive more loads than the AI. The API module consists of a three-way diode positive AND circuit followed by a saturating transistor power inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 extends the AND fan-in by connecting it to the common anode diodes of the FDD module.

Pins 8 and 9 are connected on the card for most applications. However, when the collectors are dotted, only one collector resistor can be connected (to retain the specified fan-out capability).

The API can drive a maximum of 14 AI/AOI, or equivalent, loads.

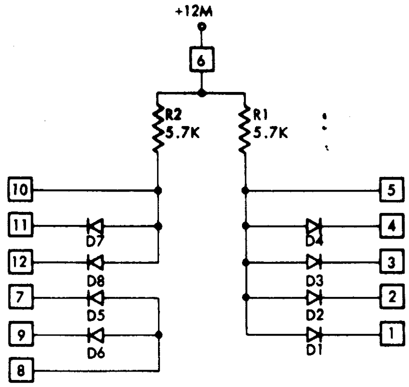
AND-OR Power Invert (AOPI)

The AOPI module (Figure 18) consists of a three-way positive AND function and one diode for an OR function followed by a saturating transistor power inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 extends the AND fan-in by connection to the common anode diodes of the FDD module. Pin 1 can extend the OR fan-in by connection to the OR diode of the $AOPX_1$ module. The maximum OR fan-in is five. The output pins, 8 and 9, are connected on the card for most applications. However, when collectors are dotted, only one collector resistor may be connected (to retain the specified fan-out capability).

The AOPI can drive a maximum of 14 AI/AOI, or equivalent, loads.

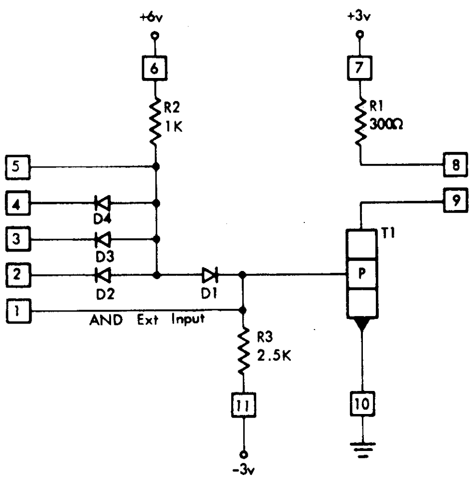
AND-OR-Invert (AOI-10)

The AOI-10 is the basic circuit of a logic family consisting of the AOI-10, AOI-10T and Line Terminator Circuits. Both the AOI-10 and AOI-10T are logic circuits with maximum fan-in of five OR inputs and five AND inputs per OR input. The AOI-10 differs from the AOI-10T only in input and delay characteristics. The AOI-10 has better delay characteristics, while the AOI-10T has a greater



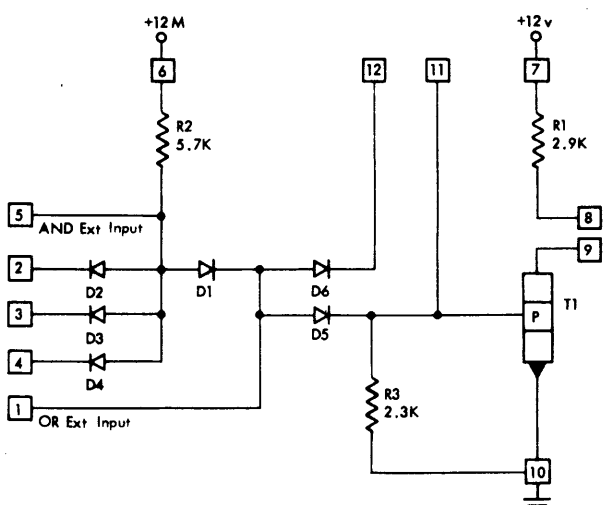
P/N361496

Figure 16. AND-OR-Power-Extend, Low-Speed (AOPX-1)



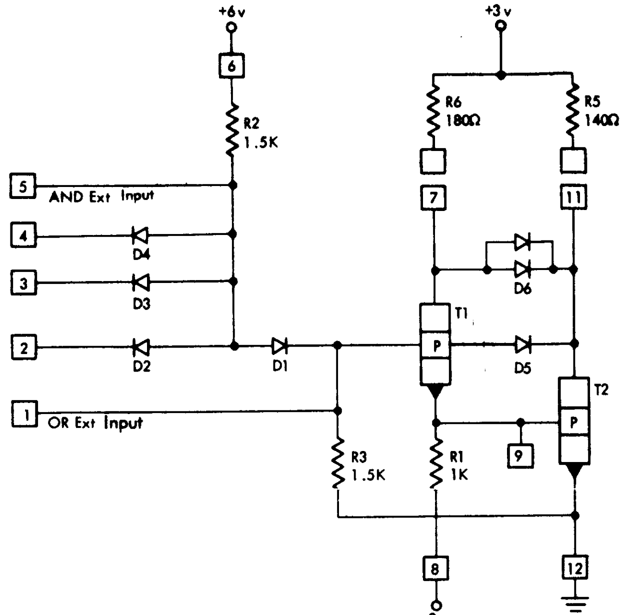
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Figure 17. AND-Power-Invert, Medium-Speed (API)



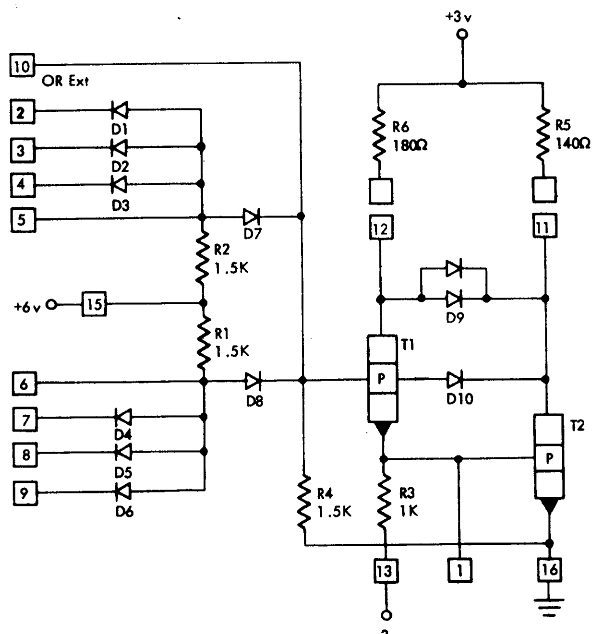
P/N 361492

Figure 18. AND-OR-Power-Invert, Low-Speed (AOPI)



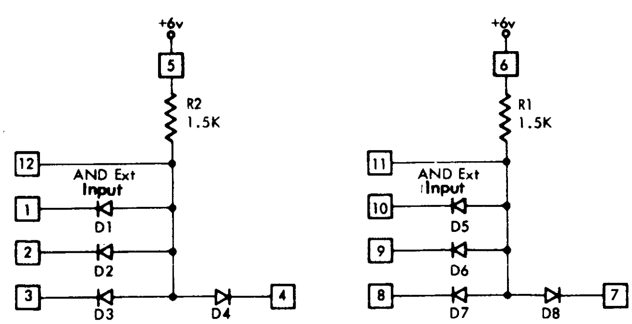
P/N 361468

Figure 19. AND-OR-Invert, High-Speed (AOI$_{10}$)



P/N 361406

Figure 20. AND-OR-Invert, High-Speed (AOI$_{10}$B)



P/N 361469

Figure 21. AND-OR-Extend, High-Speed (AOX$_{10}$)

positive-going noise rejection level. The AOI-10 is used when block-to-block wiring lengths do not exceed twelve inches. The AOI-10T is used when long line lengths or certain logical situations require a greater positive-going noise rejection level.

The output characteristics of the AOI-10 and AOI-10T circuits are identical. Both circuits have maximum fan-outs of ten AOI-10 or AOI-10T circuits. Either circuit can drive a 93-ohm transmission line terminated by an LTN or LSA. Outputs of both the AOI-10 or AOI-10T can be wired together to perform a negative OR function.

The AOI-10 circuit uses the 12-pin AOI-10 module (Figure 37) or the 16-pin AOI-10B module (Figure 38). The 12-pin AOI-10 module has one OR gate containing three positive AND diode inputs. The 16 pin AOI-10B module contains a two-way OR gate with each OR gate having three positive AND diode inputs. Each module has an OR-extend pin and an AND-extend pin.

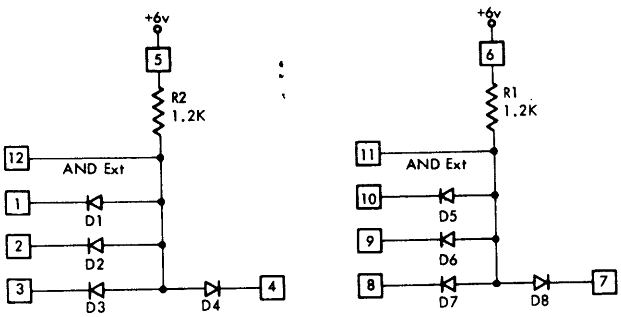
The AOX-10 module (Figure 21) is used to extend the OR function of the AOI-10 circuit. The FDD-10 module (Figure 41) is used to extend the AND function of the AOI-10 circuit. In addition, the diodes on the AOX-10 (Figure 21) and AOX-10T (Figure 40) modules may be used to extend the AND function.

AND-OR Invert (AOI-10T)

The AOI-10T circuit provides the same system function as the AOI-10 circuit, except that an additional diode level shift is incorporated to give the circuit additional immunity to positive noise pulses. It may be used in line terminator applications and other system locations requiring greater immunity to positive noise than the AOI-10 circuit provides.

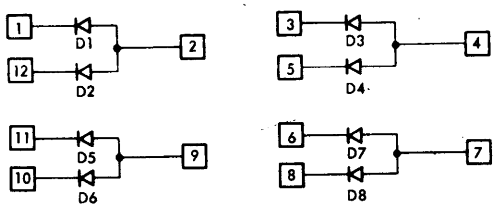
The AOI-10T circuit uses either the 12-pin AOI-10T (Figure 24) module or the 16-pin AOI-10BT module (Figure 25) plus an external resistor package containing the collector resistors R_5 and R_6.

The AOI-10T module consists of a three-input positive AND diode gate, followed by a single OR diode, a level-shifting diode pair and a nonsaturating inverter amplifier. The basic three-way AND function can be extended by connecting the diodes of the FDD-10 module to the AND extend input (pin 5) of the AOI-10T module. The AOX-10 (Figure 21) or AOX-10T (Figure 22) modules may be used for the same purpose if pins 5 and 6 are not connected to +6v. The trivial one-way OR function of the AOI-10T module may be extended by connecting the AOI-10T module to pin 1 of the AOI-10T module. The OR function can also be extended by connecting an AOX-10 module to pin 10. However, in this case the level shift diode pair is bypassed. Therefore, the input legs so involved do not have the extra noise immunity.



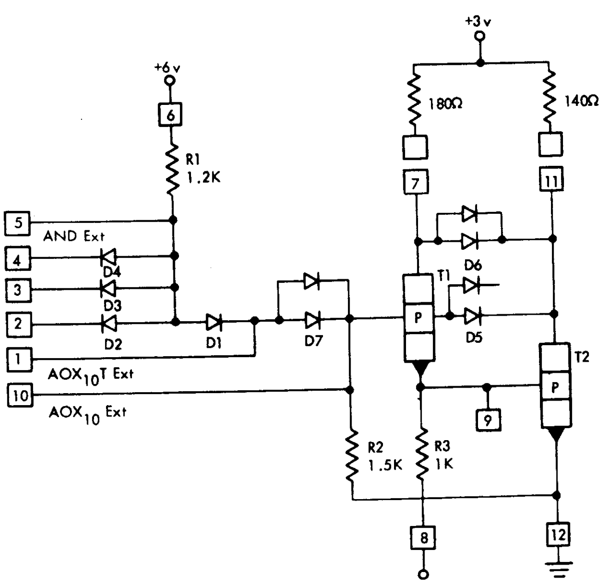
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Figure 22. AND-OR-Extend Terminate, High-Speed ($AOX_{10}T$)



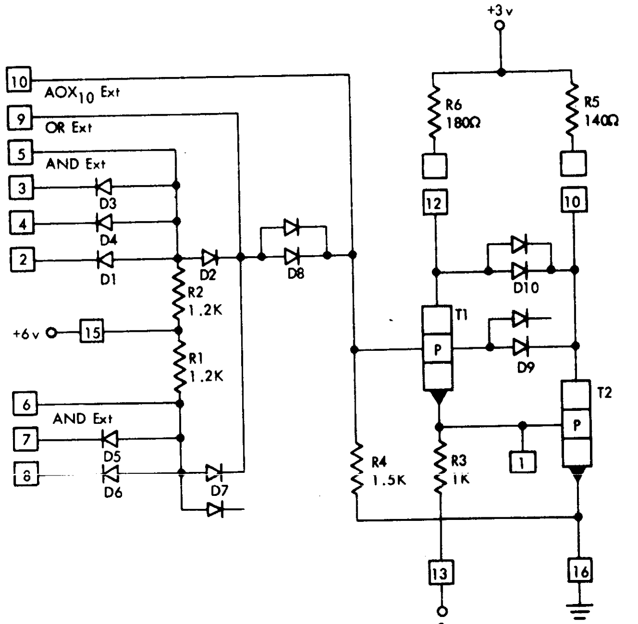
P/N 361482

Figure 23. Four Double Diodes, High-Speed (FDD)



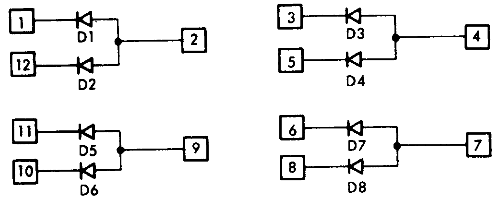
P/N 361404

Figure 24. AND-OR-Inverter-Terminate, High-Speed ($AOI_{10}T$)



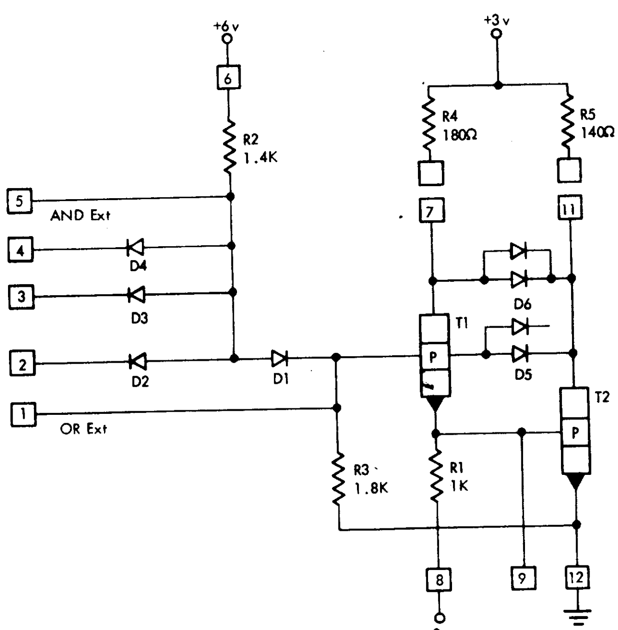
P/N 361407

Figure 25. AND-OR-Invert, High-Speed ($AOI_{10}BT$)



P/N 361414

Figure 26. Four Double Diodes (FDD_{11})



P/N 361408

Figure 27. AND-OR-Invert, High-Speed (AOI_{11})

The AOI-10BT module is identical to the AOI-10T, except that an extra AND-OR leg is provided to make it a two-way OR as compared to a trivial one way OR for the AOI-10T. Also the AND gate on this extra leg is only two way, as compared to three-way for the other leg as on the AOI-10T. The basic AND-OR capability may be extended in the same manner as the AOI-10T.

The fan-in for the AND and OR functions is limited to five each. Fan-out is limited to 10. Circuit outputs may be wired together.

AND-OR Invert (AOI-11)

The AOI-11 circuits are similar to the AOI-10 circuits. Differences are in speed and in some component values. The circuits that make up the AOI-11 circuits are: FDD 11 (Figure 26), AOI-11 (Figure 27), AOI-11B (Figure 28), AOI-11T (Figure 29), AOI-11BT(Figure 30), and AOX-11 (Figure 31).

Line Terminator Circuits (AOI-10 Circuit Family)

The LTN circuit (Figure 32) consists of a single terminating resistor (four different values) connected at the end of the line and returned to +3 volts. The resistors are discrete components places immediately at the end of the line with one to four AOI-10 circuits. Essentially, the LTN allows the line to be terminated in a logic block without the insertion of an active buffering circuit.

The Line Sensing Amplifier (LSA) line termination consists of a resistor network at the end of the line and one to ten LSA circuits placed at the end of the line or distributed along the line. Each LSA may drive only one AOI-10 circuit.

The 93-ohm programmable delay line has two main 125 nanosecond sections. Each may be programmed in increments of 5, 10, 20, 40, or 50 nanoseconds.

The transmission lines discussed are SLT printed wire, SLT flat cable, or commercial coax. All have approximately a 93-ohm characteristic impedance including the delay line.

Direct-Coupled Invert (DCI)

The DCI module (Figure 33) contains two separate direct-coupled inverters. These inverters are designed to provide a fast, economical way of extending the fan-out of an AI, or an AOI module by approximately a factor of 3. The lead between the AI or AOI output pin 9 and the DCI input pin 5 or 12 must be kept as short as possible for the full speed capability of this circuit to be realized.

The collector resistor must be connected on the driving AI or AOI to provide the necessary base current drive to the DCI. The DCI collector resistor has been left programmable, but must be connected on the card for the intended use of this module. Connect pin 2 to 3 and pin 8 to 9.

The circuit will not drive long transmission lines because of fast output transitions.

Delay Line, Driver and Terminator (DLD)

The DLD (Figure 34) consists of (1) An API driver, (2) A programmable delay line, (3) A Line Terminating Network (LTN), and (4) An AOI output stage. The output pulse width is the same as the input pulse width, but is delayed for a selected time interval.

The API line driver accepts the LTN current plus the AOI drive current, a total of 29 ma. Note that the API collector resistor is not used.

The programmable delay lines offer delays of 5-500 nsec maximum in 5 nsec increments, or four separate 5-125 nsec maximum delay lines used individually. The Line Terminating Network (LTN) with the ON input impedance of the AOI matches the characteristic impedance of the delay line (93 ohms). The AOI with the LTN acts as a terminator and as an output stage.

Direct-Coupled Invert (DCI) and Transmission Line Driver (TLD)

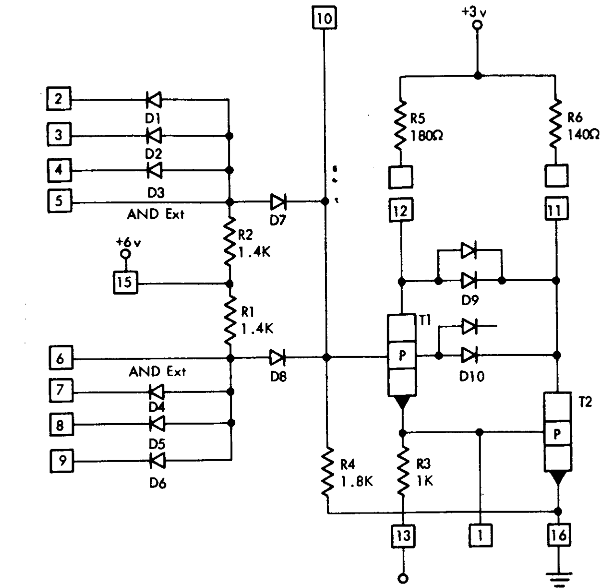
The DCI module (Figure 35) contains two separate direct-coupled inverters. The inverters are designed to provide a fast, economical way of extending the fan-out of an AI or an AOI module by approximately a factor of 4.

A DCI stage, when driven by API/AOPI, serves as a 56 ma transmission line driver (TLD).

The collector resistor must be connected on the driver in order to provide the necessary DCI or TLD base current.

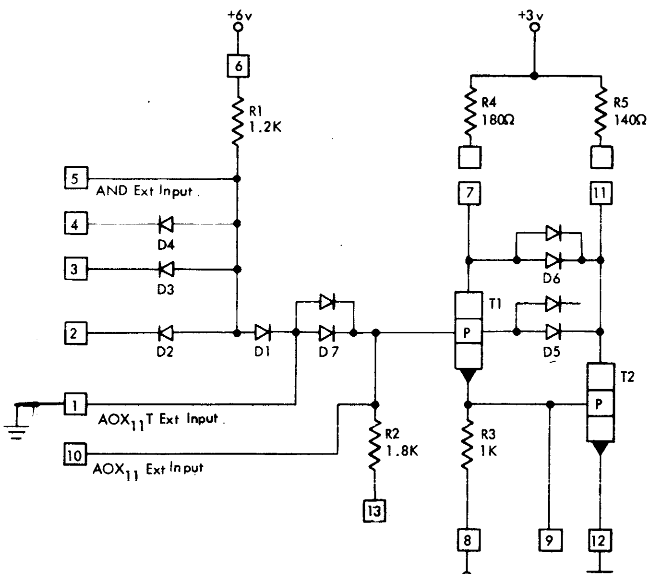
The collector load resistor of the DCI/TLD is programmable. For most applications, module pins 2 and 3 or 8 and 9 are connected on the card.

NOTE: Except for external connections, the DCI/TLD is identical to the Isolating Inverter I I (Figure 45).



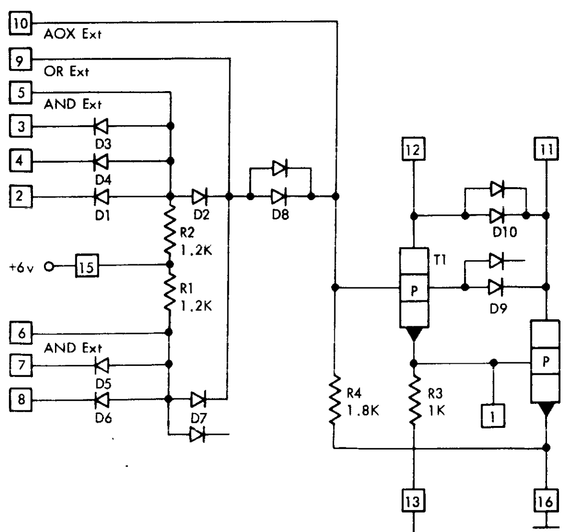
P/N 361412

Figure 28. AND-OR-Invert (Two-Way OR), High-Speed ($AOI_{11}B$)



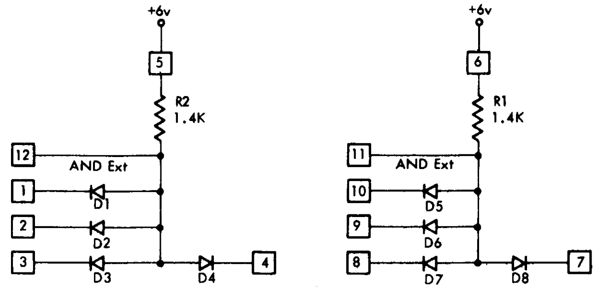
P/N 361410

Figure 29. AND-OR-Invert-Terminate, High-Speed ($AOI_{11}T$)



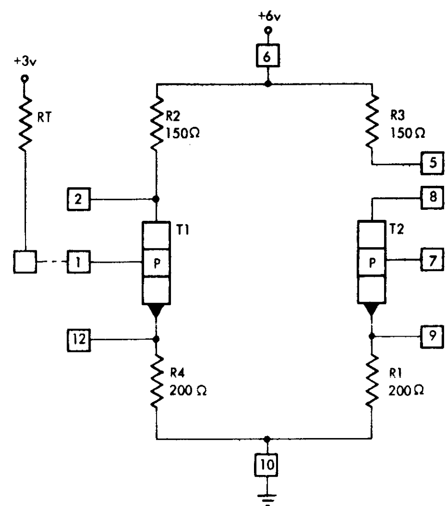
P/N 361413

Figure 30. AND-OR-Invert, High-Speed ($AOI_{11}BT$)



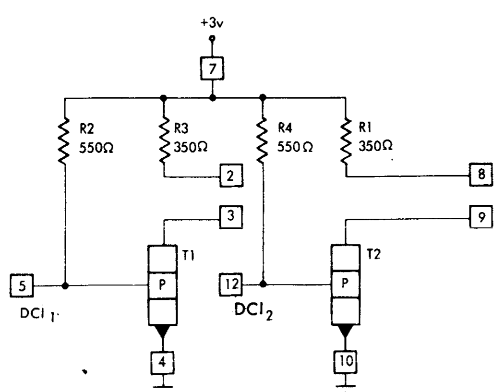
P/N 361409

Figure 31. AND-OR-Extend, High-Speed (AOX_{11})



P/N 361476

Figure 32. Line Sense Amplifier Medium-Speed (LSA)



P/N 361454

Figure 33. Direct Coupled Invert, Medium-Speed (DCI)

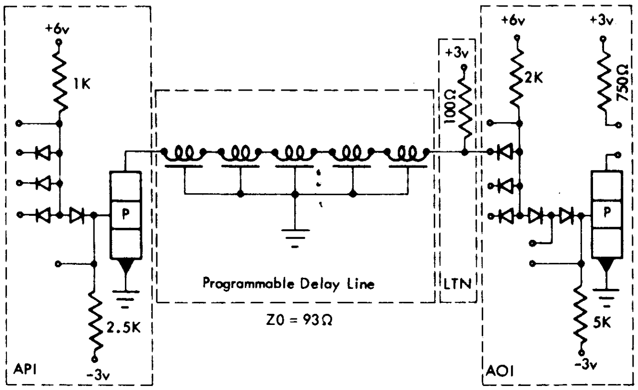
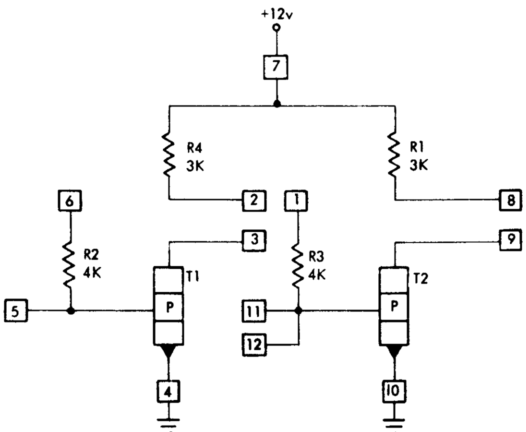


Figure 34. Delay Line Driver and Terminator (DLD)



P/N 361494

Figure 35. Direct Coupled Invert, Low-Speed (DCI)

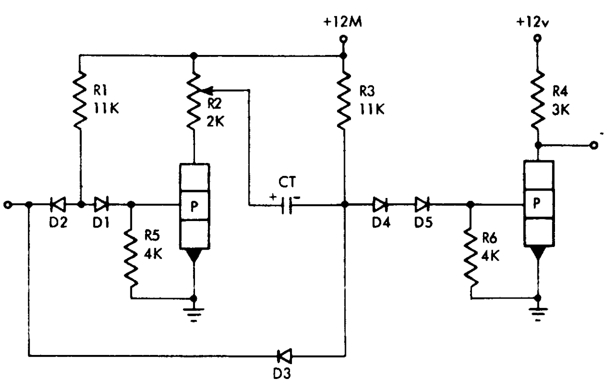


Figure 36. Delay Circuit (DLY)

Capacitor		Turn-On Delay			
0.00068	uf	1.4	-	5.5	usec
0.0018	uf	4.5	-	14.6	usec
0.0047	uf	12	-	38	usec
0.012	uf	30	-	97	usec
0.033	uf	83	-	260	usec
0.082	uf	205	-	660	usec
0.22	uf	550	-	1,780	usec
0.56	uf	1.4	-	4.5	ms
1.5	uf	3.7	-	12	ms
3.9	uf	9.7	-	31	ms
10	uf	25	-	81	ms
27	uf	67	-	220	ms

Figure 37. Timing Capacitors (DLY)

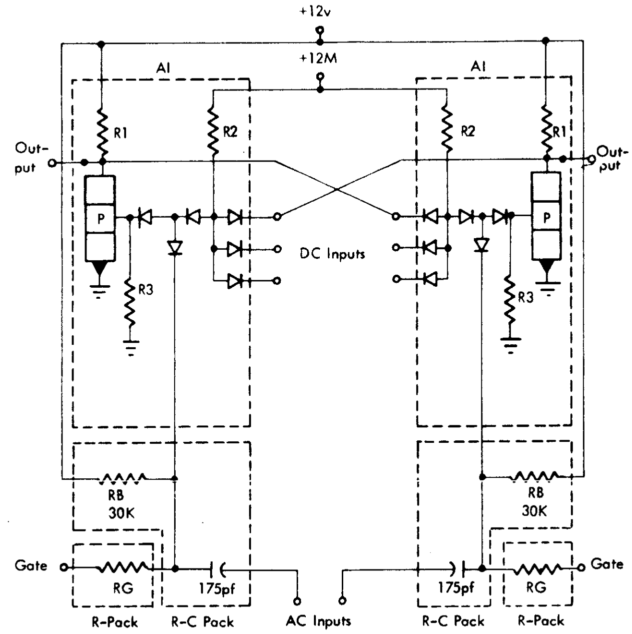


Figure 38. Flip Flop (FF)

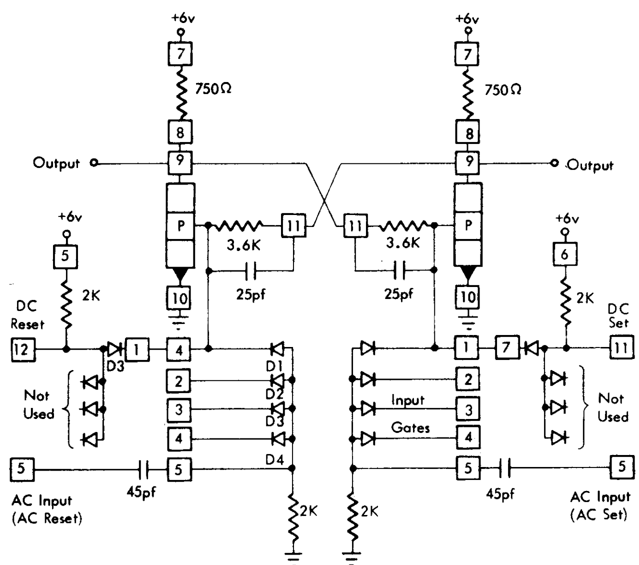


Figure 39. AC Trigger (ACT)

Delay Circuit (DLY)

Variable Delay Circuit. The delay circuit (Figure 36) consists of one AOX_1 module, one I I module, one potentiometer and one capacitor. It has a fan-in of 1 and fan-out of 5 AI's. The circuit functions as an inverter with worst case turn-off delay of 520 nsec and variable turn-on delay, ranging from 1.9 usec to 220 ms controlled by the 2K potentiometer and the timing capacitor. For a given timing capacitor, the range of the turn-on delay is fixed (Figure 37). A continuous variation can be obtained by adjusting the potentiometer. After the circuit is turned off, a minimum time must be allowed for the timing capacitor to charge up fully before it can be turned on. Otherwise, incorrect turn-on delay will result.

Fixed Delay Circuit. An R-C module combines with one AOX_1 module and one I I module to form a delay circuit with a fixed turn-on delay of 2.8 usec or 5.6 usec ±30 percent.

The module contains two resistors and one capacitor. The interconnections between modules remain as shown except that the R-C module is used to replace the 2K trim potentiometer and the timing capacitor.

Flip Flop (FFL)

The FFL (Figure 38) consists of two cross-coupled AI modules, an R-C pack and an R-pack. The AI's are fed at the cathode of D6 through a 175 pf capacitor from the negative going transition of an AC set pulse at the AC input. During the negative transition, currents from the AND resistor of the ON transistor and 30K bias resistor are directed into the collector of the AC set driver. This forces the ON transistor off. As a result other transistors will turn on.

Each side of the FFL has two DC Set/Reset inputs available which can be driven from any low-speed logic block.

Collector resistors of AI's must not be programmed. Two AI's, an R-C pack and an R-pack all must be mounted on the same card.

AC Trigger (ACT)

The AC trigger (ACT) (Figure 39) consists of two AI modules, one AOX module and a four-capacitor C-pak. Additional components may be added to increase flexibility.

The cross-coupled inverters are fed at their respective bases either from the up level of a DC set pulse (at a DC set or DC reset input), or from the positive going edge of an AC set pulse (at the AC inputs).

The current from an AC set pulse is directed either into the base of a transistor in the cross-coupled latch or is bypassed through a gate diode as determined by the voltage at the cathode of this diode. If the cathodes of the three gate diodes associated with a common AC input are at an "up level" (+3v), current from the AC input will start trigger switching by turning the transistor, connected to this gate network, from off to on. If the cathode of any one gate diode is tied to a saturated collector (0.3v), the AC input current for the gate will be sent to the gate diode through the saturated collector to ground, preventing trigger switching.

The DC set and reset inputs (11) and (12) can be driven from any 30 nsec logic block. It is impossible to program collector resistors as in other 30 nsec circuits. The number of inputs for each side of the AC trigger is:

AC inputs -- 1.

Input Gates available for use with each AC input -- 3.

DC input -- 1.

High Power Driver (HPD)

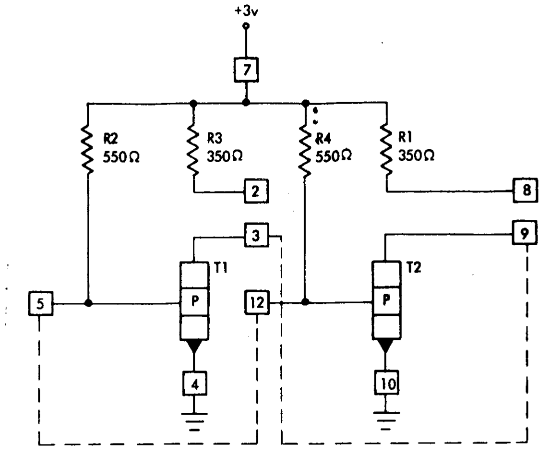
NOTE:

1. This is not a standard application of the DCI Module. The HPD is a selected DCI that has closely matched transistors to allow parallel operation of the two inverters.
2. The collector current can become 80 ma for the most unbalanced transistor pair.
3. The HPD module may not be used as a DCI.

The HPD (Figure 40) is a high-current driver made by connecting the two inverters in parallel on a specially selected DCI module. The HPD can be driven by an AI or an AOI if the collector resistor on the driving block is returned to +6v. The HPD is mounted in the adjacent module position.

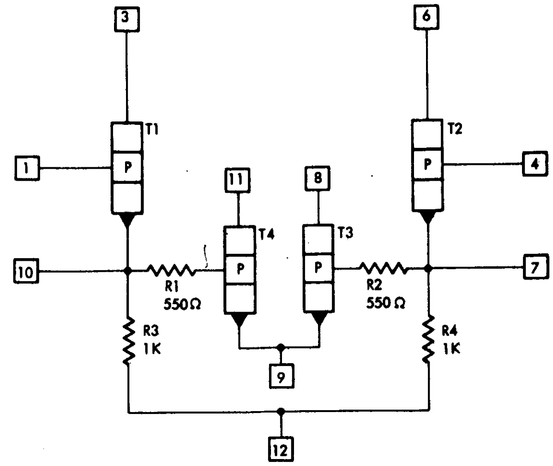
The API-3v can also drive the HPD with normal power supplies.

The HPD may be used to drive a large number of loads (36 AI or 28 AOI) or it may drive long transmission lines. The HPD may not be used to drive both LSA's and regular loads simultaneously. The HPD cannot drive long lines when it is driving a high fan-out of AI's, etc., because of the reflections on the unterminated transmission lines.



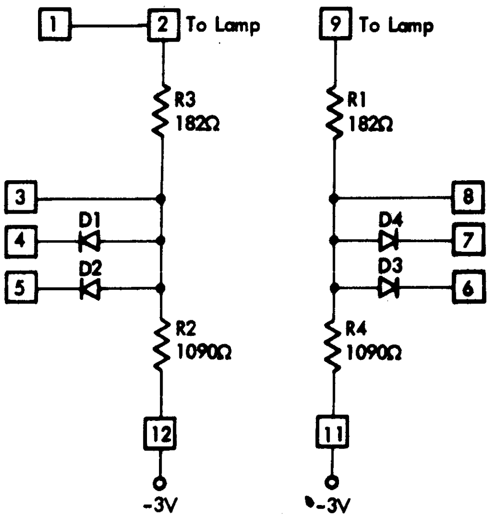
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Figure 40. High Power Driver (HPD)



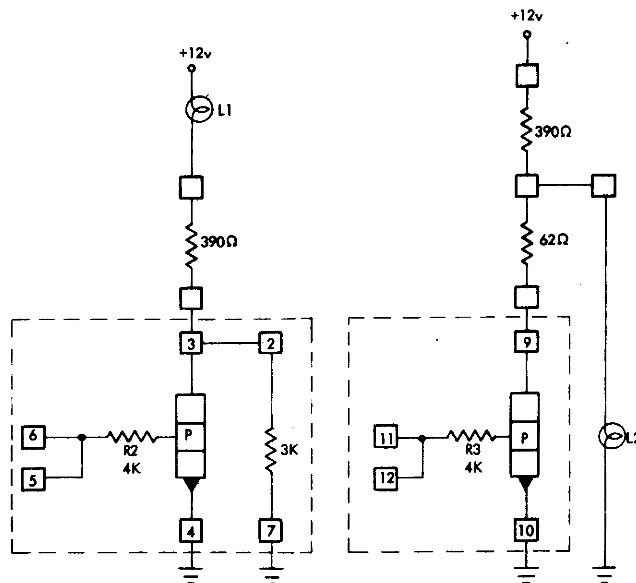
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Figure 43. Indicator Driver, 240 ma (ID)



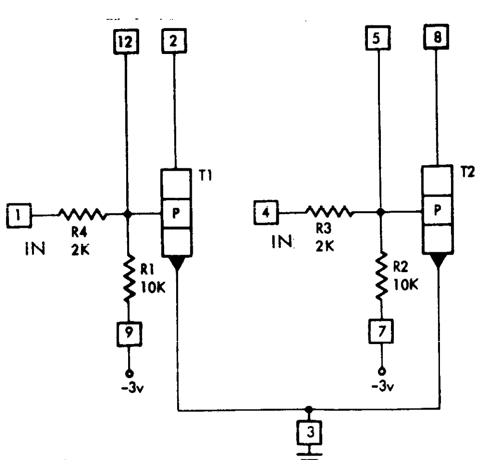
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Figure 41. Indicator Coupling Network (ICN)



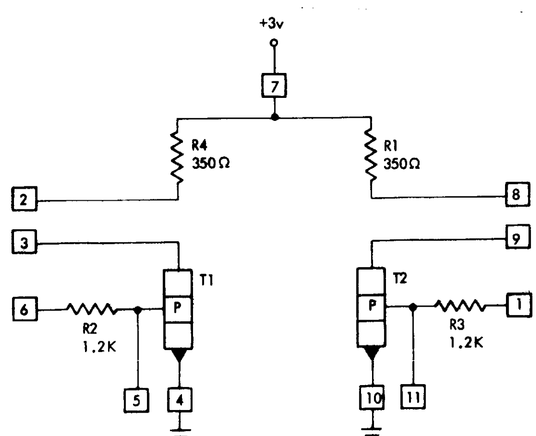
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Figure 44. Indicator Driver (IDL)



P/N 361480

Figure 42. Indicator Driver, High-Speed (ID)



P/N 361479

Figure 45. Isolating Inverter, Medium-Speed (II)

Indicator Coupling Network (ICN)

The indicator coupling network (Figure 41) is used in conjunction with a 3v, 9 ma incandescent lamp. One end of the lamp is returned to +6 volts and the other end to R_1 of the coupling network.

The lamp glows when the driving collector is down. Thus, the lamp will glow when all of the AND circuit inputs are up on the driving block. The coupling network draws the same current as two logic loads. Three logic blocks and one indicator may be driven from a logic block.

The lamp may be located remote from the coupling network.

Indicator Driver (ID)

The indicator shows evidence of the output state of the driving circuit. For the up level indicator, lamp L_1 is on only when the driving circuit is at an up level. For the down level indicator, lamp L_2 is on only when the driving circuit is at a down level.

Because of the high input impedance (2K), neither circuit (when used individually) loads down the driver (Figure 42). As a general rule, no two indicators should be driven from the same driver. However, the driver may drive the regular AND logic blocks plus an ID.

40-ma Switch (Indicator Driver) (ID_2)

The 40-ma switch (Figure 43) is a driver capable of accepting 40 ma at its output. It is used in slow speed applications such as an indicator driver.

The ID_2 may be driven by high, medium, or low-speed circuits. Its driver may drive the regular AND blocks and the ID_2 block. It cannot be driven from an LSA.

Indicator Driver (IDL)

An I I stage (a saturating transistor) (Figure 44) serves as a driver for both the up and down level indicators.

The bulb, when lit, indicates the state of the input level. The up level indicator requires a 1 and the down level indicator a 0 at the input to turn the light on.

Because of the high input impedance of the I I the driver can drive its full load plus the indicator driver (ID).

The indicator driver, besides driving either of the indicators (bulbs), can also drive an API/AOPI load for latch-back (transient noise indication).

Using one II/DCI module, two "R-Paks," and two bulbs, these combinations are possible:

1. Two up-level indicators.
2. Two down level indicators.
3. One up and one down level indicator.

The following special conditions apply for the IDL:

1. The indicator driver(s) must not be used as a link in a logic chain.
2. II /DCI or XOI loads must not be driven by IDL's.
3. The indicator driver(s) can drive, besides the bulb and its network, an additional AI/AOI or API/AOPI load only for latch-back purposes.

Isolating Inverter (II)

The II module (Figure 45) consists of two isolating inverters. Because of the current-limiting resistor in the base, the II fan-out capability is only 7 AI/AOI, or equivalent, loads.

Pins 1 and 6 are the input pins and pins 2, 3 and 8, 9 are the output pins. Pins 2, 3 and 8, 9 may be connected on the card for most applications. When the collectors are dotted, only one collector load resistor is connected to retain the specified fan-out capability.

Sample Pulse Driver (SPD)

The SPD (Figure 46) consists of one-half of a DCI, one-half of an FDD, one-half of a TTX and a pulse transformer. The input to the SPD can be an AI, AOI, or API minus the collector resistor. When the input is at the up level, T_1 is turned on and current is built up in the primary inductance L_1 with a time constant of L_1/R_1. During the time that T_1 is on, T_2 remains off. When the input is at the down-level, T_1 switches off. The current in the primary inductance falls at a rate of di_1/dt, and T_2 is turned on by the mutual coupling in the transformer. When T_2 is turned on, a large current is delivered to the load.

The diodes at the collector of T_2 limit the voltage swing, while the diodes between the collector of T_1 and the emitter of T_2 are used for the off current from the AC inputs. The SPD must drive at least 16 AC inputs on two separate lines of no more than 10 inches each when the output of the SPD has no load resistor. When only two AC inputs are used, the output of the SPD must be terminated with a 50-ohm resistor. The SPD can drive 20 AC inputs when the output is not terminated. The output of

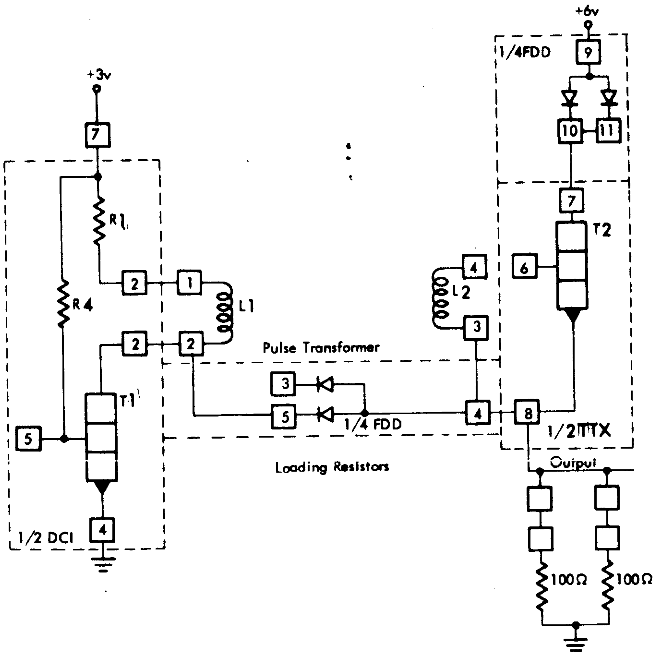


Figure 46 Sample Pulse Driver, Medium-Speed (SPD)

Capacitor	Output Pulse Width
0.00068 uf	0.99 - 5.1 us
0.0018 uf	3.4 - 13.5 us
0.0047 uf	9 - 35 us
0.012 uf	23 - 90 us
0.033 uf	62 - 248 us
0.082 uf	153 - 615 us
0.22 uf	410 - 1,650 us
0.56 uf	1.1 - 4.2 ms
1.5 uf	2.8 - 11 ms
3.9 uf	7.3 - 29 ms
10 uf	19 - 75 ms
27 uf	50 - 200 ms

Figure 49 SSL Timing Capacitors

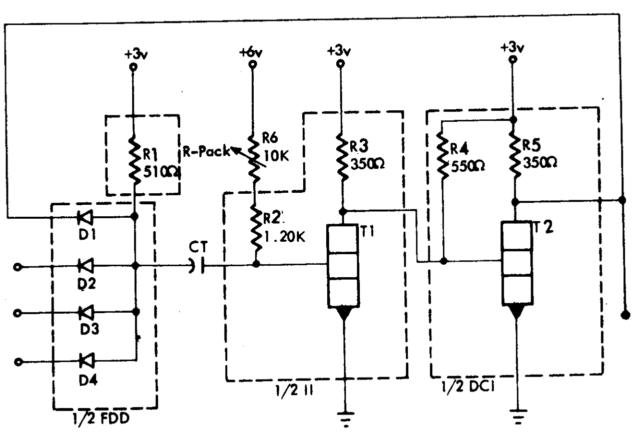


Figure 47 Singleshot, Medium-Speed (SSA)

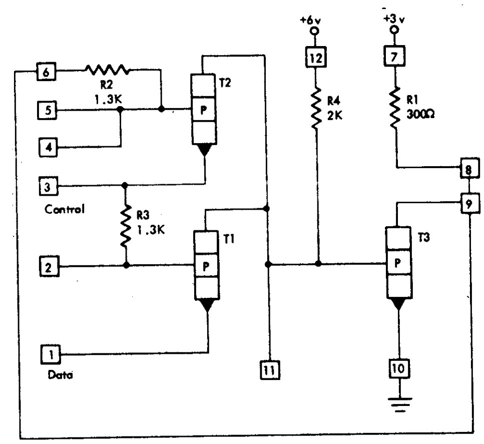


Figure 50 Exclusive OR Latch, Medium-Speed (XORL)

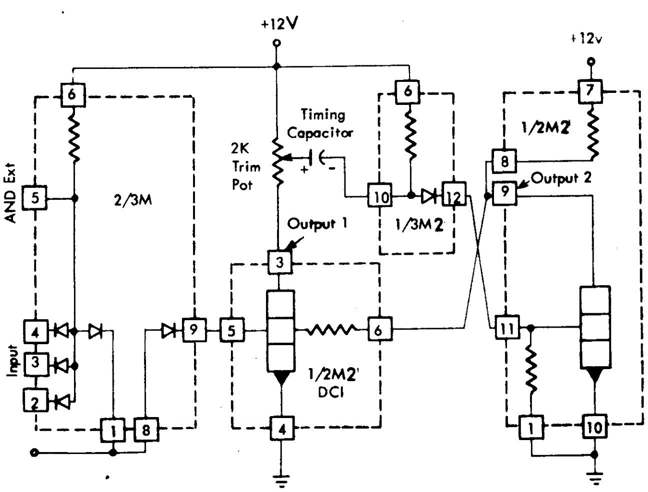


Figure 48 Singleshot, Low-Speed (SSL)

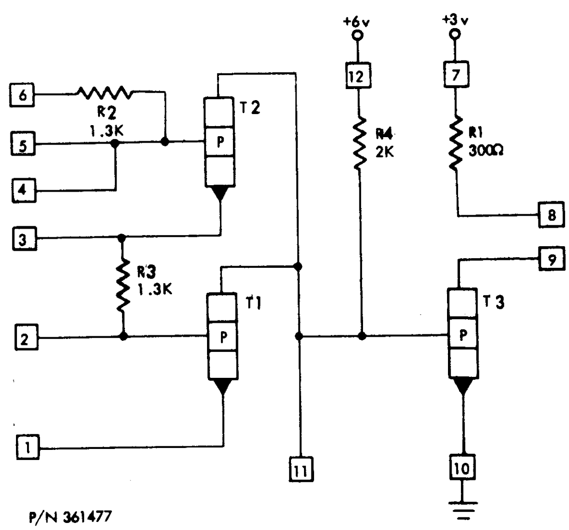


Figure 51 Exclusive OR, Medium-Speed (XOR)

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the SPD is an emitter follower, and the impedance reflected back to the emitter decreases as the number of AC inputs increases.

Single-Shot (SSA)

The SSA (Figure 47) uses one AI module, one-half of a DCI module, one-half of an AOX module, a trim potentiometer, and a timing capacitor. However, the AI module is not used as an AND inverter: it is used solely to provide a transistor and two resistors. The AND diodes of the AI module are not used, the translate diode is shorted and the 3.6K and the 2K resistors are paralleled (see Figure 47). The output pulse is controlled by the 10K trim potentiometer and the timing capacitor, C_T. For a given C_T, the range of the output pulse width is fixed, and by means of the trim potentiometer, a continuous variation can be obtained.

Single-shot (SSL)

Variable Single-shot. The single-shot (Figure 48) consists of one AOX_1 module, one II module, one trim potentiometer and one capacitor. D_2, D_3, D_4 are AND fan-in's. The fan-in can be extended by using FDD or AOX modules.

A positive transition triggers the single-shot. It has two outputs which are complementary to each other with output 2 in phase with the input. The output pulse width is controlled by the 2K trim potentiometer and the timing capacitor. For a given timing capacitor, the range of the output pulse width is fixed (Figure 49). By adjusting the trim potentiometer, a continuous variation can be obtained.

Between the end of the output pulse and the start of the next trigger, a minimum time (recovery time is equal to or greater than the desired output pulse width) must be allowed for the timing capacitor to be fully charged, or a "premature" triggering will result in an incorrect output pulse width.

NOTE: Output 1 is a negative-going pulse and output 2 is a positive-going pulse. The single-shot cannot drive a DCI or II. Output 1 cannot be used if the input pulse width is longer than the desired output pulse width.

Fixed Single-shot. An R-C module combines with one AOX_1 module and one II module to form a single-shot with fixed pulse width of 2.8 usec or 5.6 usec $\pm$30 percent. The module contains two resistors and one capacitor. The interconnections between modules remain as shown in the preceding description, except that the R-C module is used to replace the 2K trim potentiometer and the timing capacitor.

Exclusive OR Latch (XORL)

The XOR Latch (Figure 50) has a single bi-stable output that can be changed by proper sequencing of the control and data inputs. The inputs can be used in either sequence 1 or sequence 2:

Sequence 1

a. Data Line Up — With the rise of the clock pulse the output will be set to the (0) state. All further changes in the control line will not affect the state of the latch.

b. Data Line Down — With the rise of the clock pulse the output will be set to the (1) state. All further changes in the control line will not affect the latch state.

Sequence 2

a. Data Line Up — With the fall of the clock pulse the output will be held in the (0) state.

b. Data Line Down — With the fall of the clock pulse the output will be held in the (1) state.

In either sequence 1 or 2, the control is normally down.

Exclusive-OR (XOR)

This circuit (Figure 51) performs the exclusive OR of the signals applied to pins 6 and 3 when pins 6 and 1 are tied together. When the inputs are both up or both down, the output will be at a potential of less than 0.30v. When the inputs are not identical (i.e., one up and one down) the output will be between 2.0v and 3.0v, depending on the loads.

The XOR module will not perform the exclusive OR latch function. The XOR-L module is the exclusive-OR latch.

Exclusive-OR-Invert (XOI)

This circuit (Figure 52) performs the exclusive-OR function of the signals sent to the input (pins 9 and 2). Connections to pins 4, 2, 5, and 10 can be made on the card. (Connectors to these pins cannot be made from the socket.) The output (pin 6) is inverted.

When the inputs are identical (i.e., both up or both down) the output will be more than +20v depending on the loads. When the inputs are not identical (i.e., one is up and one is down) the output will be less than +0.29v.

The XOI can drive 7 AI/AOI, or equivalent, loads.

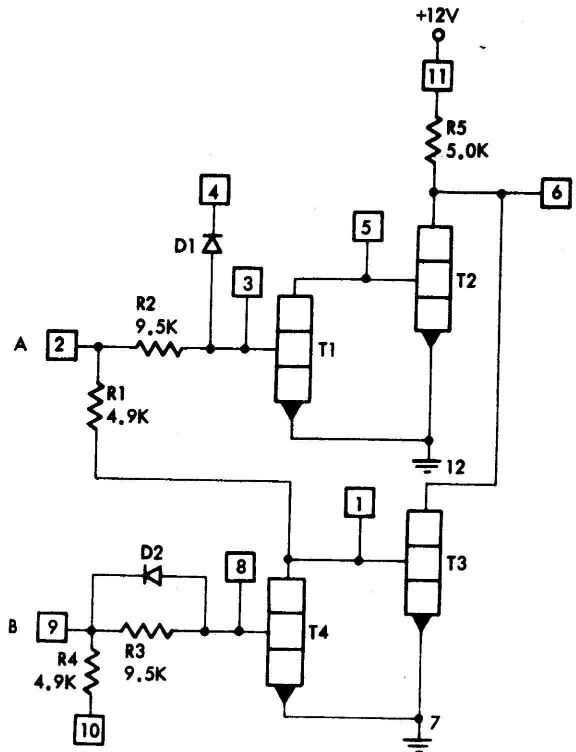


Figure 52. Exclusive-or-Invert, Low Speed (XOI)

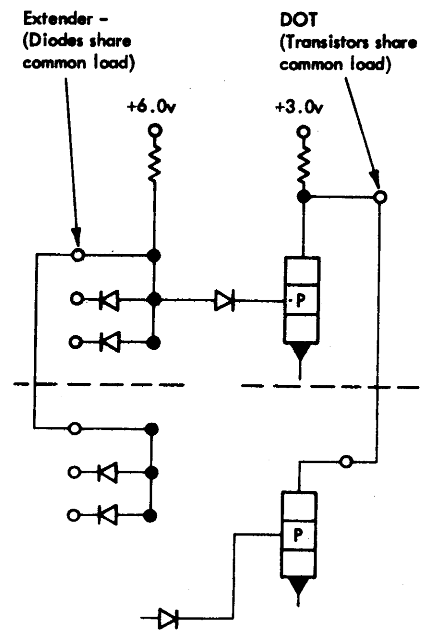


Figure 54. Typical Extender Circuit

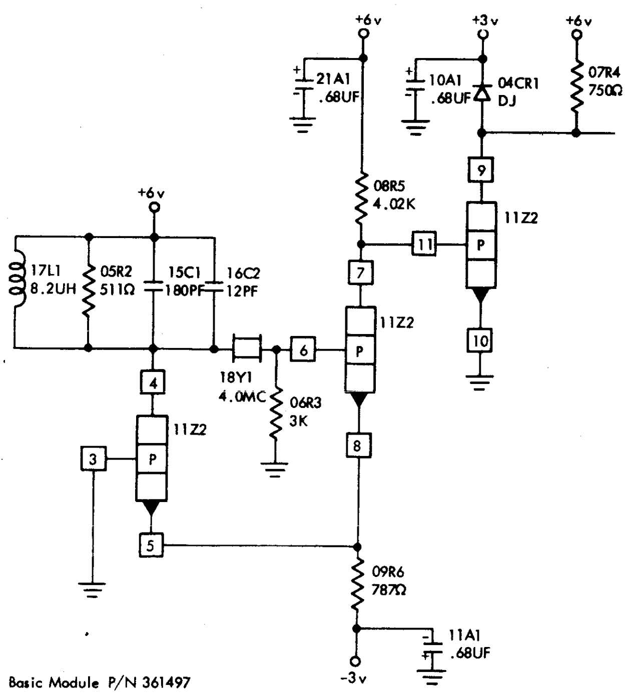


Figure 53. Crystal Oscillator

Crystal Oscillator (OSC)

The free-running crystal oscillator (Figure 53) serves as a pulse generator. The oscillator produces pulses or voltage variations of a definite frequency, e.g., 4.0 mc. The circuit consists of a basic switching circuit whose output is determined by the quartz crystal. The crystal vibrates at 4.0 mc and develops a sinusoidal voltage that is amplified and clipped to produce the square wave output of the oscillator. The inductively tuned tank circuit provides regenerative feedback to sustain the crystal oscillations.

Extender (E) and DOT Functions

AND circuits and OR circuits may be connected together to produce a single output (Figure 54). When the circuit of the AND or OR block is diode logic, one logic block is connected to the other by an extender (E). The extender (E) is, in effect, a method of adding diodes to the input of a circuit. The extender symbol (E) is only used on the ALD's when the connection is made between two cards.

When the output of the AND or OR block comes from a transistor (vs a diode) the logic blocks are connected with the DOT block (Figures 55 and 56). The DOT block is simply wiring connecting the outputs of two or more transistors.

The function of the DOT block depends upon the desired logical use of the shared transistors. Generally, the AND DOT is a +A; the OR DOT is a -OR.

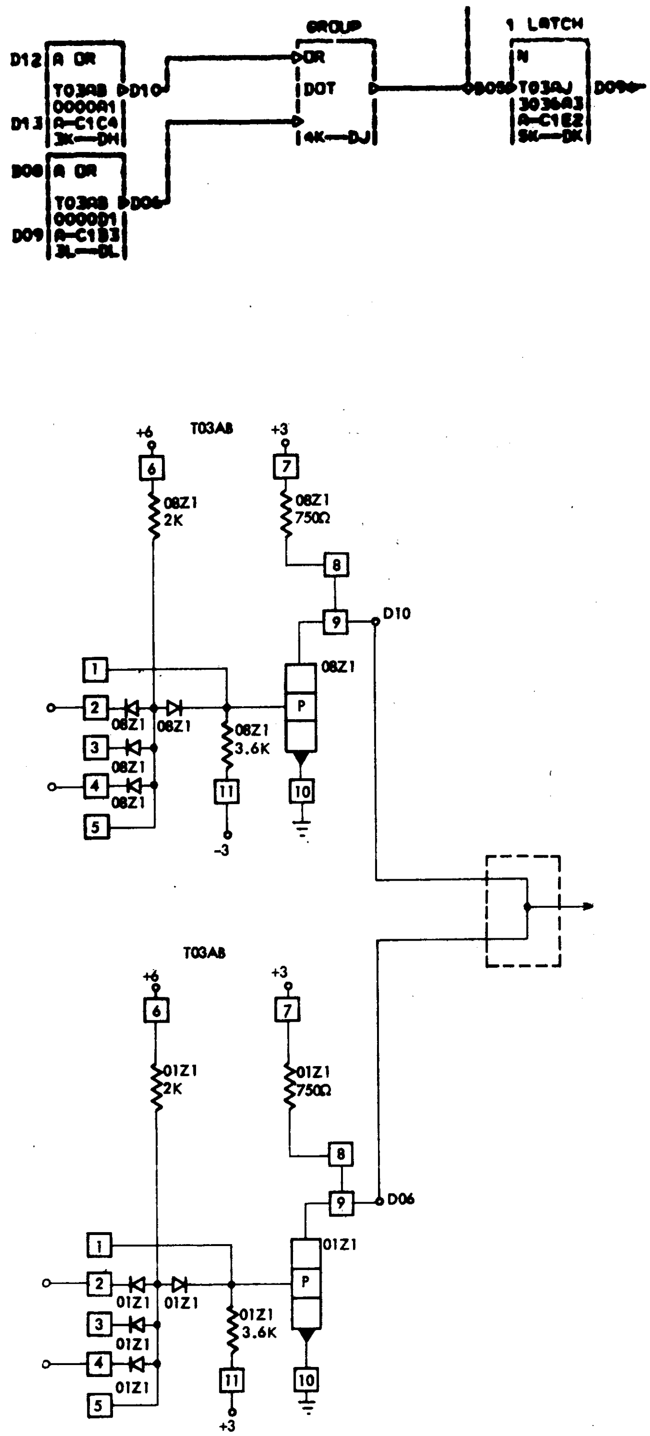


Figure 55. The OR DOT Block

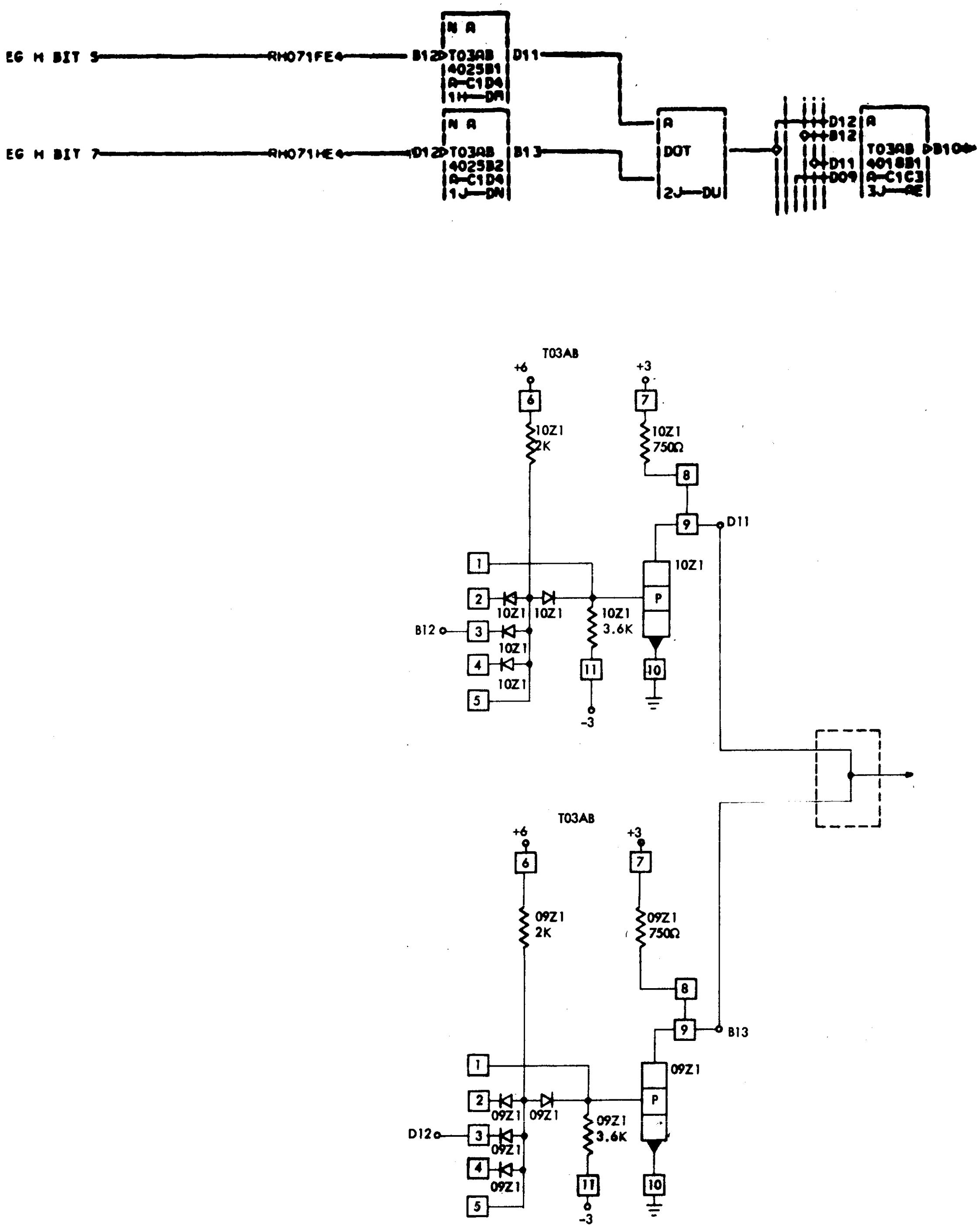


Figure 56. The AND DOT Block

CIRCUIT FLYER LISTING

(By Block Identification Number)

The Block Identification Number or Circuit Number is the coded name given to a particular circuit. This number can be found in a cross-reference called the "Circuit Flyer Title and Specification" list. (See Figure 106.) This list contains all circuit numbers in alphanumeric order and calls out all the circuit flyers associated with the block identification or circuit number. In the logic block configuration, this number will always be found inside the block on the third line.

The following list presents representative circuit groupings from the "Circuit Flyer Title and Specification" list.

Circuit Number	Title
T03AA	AI/No Load
T03AB	AI/750-ohm Load
T03AC	AND
T03AD	OI/No Load
T03AE	OI/750-ohm Load
T03AF	API/No Load
T03AH	Decoder Terminator
T03AI	Exclusive-OR/Loaded
T03AJ	API/300-ohm Load
T03AK	Exclusive-OR Latch
T03AO	7-Way API/300-ohm Load
T03AQ	AND/Multiplex Interface Driver
T03AR	Multiplex Interface Driver
T03BN	Gate
T03BO	Minus OR Invert/Loaded
T03BP	Decoder
T03BR	Sense Strobe AND
T03BS	Sense Amplifier AND
T03BV	Extended API
T03BW	Extended API/270-ohm Load
T03CE	AND Gate
T03SG	AND Invert
U03AA	AND
U03AC	Z Termination
U03AD	AND Invert/No Load
U03AE	OR Invert/Loaded
U03AF	AND Invert/Loaded
U03AG	4-Way Exclusive OR
U03AH	8-Way Exclusive OR
U03AI	AND

U03AJ	OR Invert/No Load
U03AK	AND Invert/No Load
U03AL	OR Invert/Loaded
U03AM	AND Invert/Loaded
U03AN	4-Way Exclusive OR
U03AO	8-Way Exclusive OR/Loaded
U03AP	AND Network to 1.2K
U03AQ	AND Invert Terminate/No Load
U03AR	AND Invert Terminate/Loaded
U03AS	OR Invert Terminate/No Load
U03AT	OR Invert Terminate/Loaded
U03AU	AND Terminate
U03AV	OR Terminate Invert/No Load
U03AW	OR Terminate Invert/Loaded
U03AX	AND Invert Terminate/No Load
U03AY	AND Invert Terminate/Loaded
U03AZ	OR Terminate Invert/No Load
U03CA	OR Terminate Invert/Loaded
U03CF	Memory Driver Gate
U03CK	OR Invert/No Load
U03CL	OR Invert/Loaded
U03CM	OIT/No Load
U03CN	OR Invert Terminate/Loaded
U03CU	OR Invert Terminate/Loaded
S05AH	Isolating Inverter
S05AM	Final Amplifier
S05AO	Delay Line Terminator
S05AP	Transmission Line Receiver (TLR)
S05AS	Isolating Inverter (II)/No Load
T05AA	Direct-Coupled Inverter/No Load
T05AB	Direct-Coupled Inverter/Loaded
T05AK	Drive Segment
T05BG	Delay Line Driver

T05BI	Driver Strobe
T05BJ	Lamp Test CCD for DLID
S06AB	Inhibit Timer
S06AE	Fix Strobe Emitter Follower
S06AK	Transmission Line Receiver (TLR)
S06AN	Transmission Line Receiver (TLR)/Loaded
T06AA	Line Sense Amplifier (LSA)
T06AD	C-9 Select Bus Driver
T06AJ	Direct-Coupled Inverter Driver
T06AK	Driver
S07AA	Preamplifier
S07AF	Sense Amplifier 2 Part A
S07AF	Sense Amplifier 2 Part B
T07BB	Paraphase Amplifier
T10BB	Sense Amplifier
T10BC	Driver Supply
T10SA	Driver Control
S11AG	Delay Line Driver
S15AK	300 ma Driver
T15AA	High Power Driver/175-ohm Load
T15AE	High Power Driver/No Load
T15AD	S-9 Write Driver
T15AQ	XY Gate or Inhibit Driver
T15AY	High Power Driver-Combined Logic
T15BC	Gate Strobe
T15BD	Up Level Indicator Driver
T15BE	Sense Strobe Driver
T15BF	Driver Supply Amplifier
T15BG	Driver Supply Output
S16AE	Z Driver
S16SA	XY Driver
S16SB	XY Driver

T16AF	S-9 Write Driver
T16AH	S-9 Read Driver
T16BB	Down-Level Indicator Driver
T20AB	400 kc Trigger
T20AD	AC Trigger No. 2
S21AA	50-60 pps Limiter
T21AU	500 nsec Single-shot
T21AV	Variable Single-shot
T21CI	410 nsec Single-shot
T21CJ	410 nsec Single-shot
S22AU	4 mc Xtal Oscillator
S22AV	2 mc Xtal Oscillator
S22CQ	10 mc Variable Frequency Oscillator
T22BC	Clock Oscillator 3.2 mc/s
O22AA	100 kc Oscillator
S25AA	Z Clamp
S25AC	Reference Voltage
S25AD	Reference Voltage
S25SD	Driver Control
T25AC	S-9 Read Driver Clamp
T25AG	Sense Level Set
T27BB	Sense Clamp Power Amplifier
T27BC	Sense Clamp
T31BC	Change-Over Switch
S32AC	Terminator Gate
S32AD	Gate Decoder
S32AE	Gate
T32AH	Core-Gate
T40AH	8-Position Clock
S45AA	Variable Delay Line
S45AD	5-125 nsec Delay Line

S45AH	Elapsed Time Meter Display
T45BB	Variable Delay Line
T45BC	Clock Delay
T55AD	15 ma Switch, Indicator Driver/No Load
T55AF	Up-Level Indicator Driver
U55AA	15 ma Switch, Indicator Driver
U55AB	40 ma Indicator Driver/No Load
U55AC	15 ma Switch, Indicator Driver/420-ohm Load
U55AD	15 ma Switch, Indicator Driver/1-Kohm Load
S60SB	Compensation Network
T60AI	+48V Integrator
T60BF	Switch Integrating Network
S61AC	Ltn - Replaced by T61AD
S61AF	Jumper
S61AO	Transmission Line Receiver
S61AP	Diode, Type 6V
S61AR	Terminating Resistor, 100-ohm
S61AU	Integrator
S61AY	Pluggable Switch
S61CB	Resistor Load
S61CC	Type DD Diode Clamp
S61CD	Type GU Diode Clamp
S61CH	500-ohm Potentiometer
S61EE	Pluggable Jumpers
S61SC	14.3-ohm Resistor
S61SZ	21-ohm Resistor
S61TB	0.68 μf Decoupling Capacitor
T61AA	750-ohm Load Resistor
T61AB	750-ohm Load Resistor
T61AC	350-ohm Load Resistor
T61AD	Line Terminate Network
T61AJ	300-ohm Load Resistor
T61AP	100-ohm Terminating Resistor

T61AU	C-9 Select Bus Terminator
T61AZ	1.5-Kohm Load Resistor
T61BD	Driver Damping Network
T61BE	Driver Collector Load
T61BF	Driver Emitter Load
T61BH	Clamp Level Supply
T61BI	Resistor Network
T61BJ	Delay Line Terminator
T61BK	75-ohm Load Resistor to -3v
T61BO	300-ohm Load Resistor to -3v
T61BP	1.8-Kohm Load Resistor to -3v
T61CD	C-9 Select Bus Terminate 2
T61CF	FDD Diode
T61CK	Resistor - Inductor
T61CL	175-ohm Load Resistor to +3v
U61AB	140-ohm Load Resistor to +3v
U61AC	125-ohm Load Resistor to +3v
U61AD	420-ohm Load Resistor to +3v
U61AE	165-ohm Load Resistor to +3v
U61AF	230-ohm Load Resistor to +3v
U61AG	180-ohm Load Resistor to +3v
U61AL	LSA Line Terminate Network (LTN)
U61AN	LSA Resistor Network
U61AP	Line Terminate Network
S63EB	Reed Relay, Point NC
S63ED	Reed Relay, Assembly 6V
S63EG	Reed Relay, Point NO
S63EH	Reed Relay, Point NC
T66BA	Real Time Clock

TABLE OF HARDWARE CONSTANTS

Capitance

Printed wiring	1.8 to 2.2 pf/inch (add 0.4 pf/inch for each adjacent line)
Flat cable	1.7 pf/inch
Paddle card	2.0 pf
Via hole	0.6 pf
Contact (small card)	3.0 pf
Transistor collector	6.0 pf
Diode	2.5 pf

Resistance

Printed wiring	0.5 Ω/ft
Flat cable	0.233 Ω/ft
Coax cable 535912	0.05 Ω/ft
Coax cable 535914	0.098 Ω/ft
Coax cable 595712	0.12 Ω/ft
Coax cable 595997	0.048 Ω/ft
Delay line (125 nsec section)	1.0 Ω
Discrete wire (#30)	0.111 Ω/ft
Serpent connector	0.04 Ω (Spec. 877223)

Delays

Printed wiring (large board)	1.96 to 2.28 nsec/ft
Printed wiring (small card)	0.156 to 0.165 nsec/ft
Discrete wire (large board)	1.3 to 1.5 nsec/ft
Flat cable	1.4 to 1.6 nsec/ft
Contact (small card)	0.12 nsec average
Cable paddle cards (laminated)	0.22 to 0.33 nsec
Cable paddle cards (non-laminated)	0.15 to 0.2 nsec
Coax cable	1.27 nsec/ft

MODULE CONFIGURATIONS (By Module Number)

Modules of several types and speeds are used in the SLT circuits. Figures 58 through 103 show the circuit configurations (with pin numbers) of the modules used. For ease in cross-referencing, the modules are listed in Figure 57 (1) by part number and type and (2) by name.

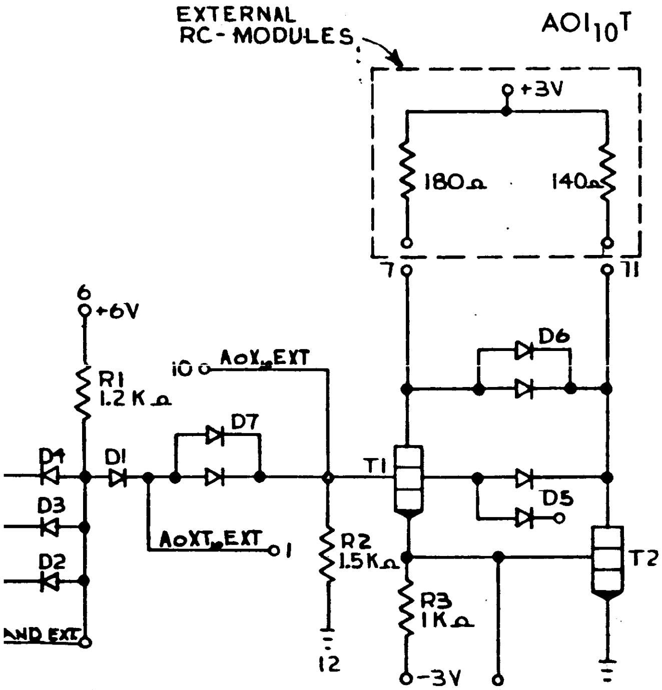
MODULES BY PART NUMBER AND TYPE

361404	AO11OT	HS
361405	AOX1OT	MS
361406	AO11OB	HS
361407	AO11OBT	HS
361408	AO111	HS
361409	AOX11	HS
361410	AO111T	HS
361411	AOX11T	HS
361412	AOX11B	HS
361413	AO11BT	HS
361414	FDD11	HS
361415	TLR	LS
361426	ID	
361427	TLR	
361429	FTX	MS
361430	FTX	
361433	FTX	
361451	AI	MS
361453	AOI	MS
361454	DCI	MS
361455	AOX	MS
361456	AOXB	MS
361457	FTX	MS
361458	TTX	
361459	FDD	MS
361468	AO11O	HS
361469	AOX1O	HS
361471	ICN	
361473	API - 3V	MS
361475	HPD	
361476	LSA	MS
361477	XOR	MS
361479	II	MS
361480	ID	HS
361482	FDD	HS
361483	FDD	MS
361486	XORL	MS
361489	AOX2	LS
361492	AOPI	LS
361493	AOI	LS
361494	DCI	LS
361495	AOXI	LS
361496	AOPX-I	LS
361497	FTX	LS
361499	FDD	LS

MODULES BY NAME

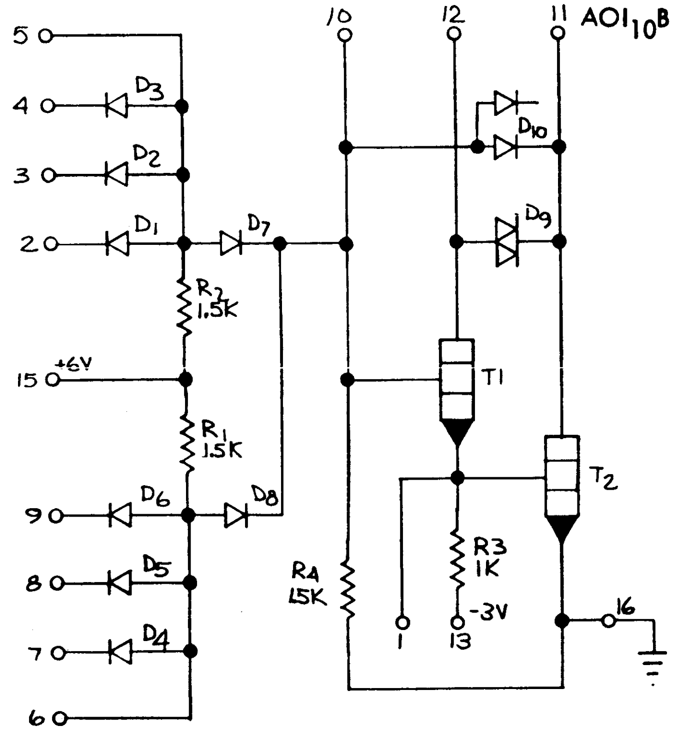
361451	AI	MS
361453	AOI	MS
361493	AOI	LS
361468	AO11O	HS
361406	AO11OB	HS
361407	AO11OBT	HS
361405	AO11OT	MS
361408	AO111	HS
361412	AO111B	HS
361413	AO111BT	HS
361410	AO111T	HS
361410	AOPI	LS
361496	AOPX-I	LS
361455	AOX	MS
361495	AOXI	LS
361469	AOX1O	HS
361404	AOX1OT	HS
361409	AOX11	HS
361411	AOX11T	HS
361456	AOXB	MS
361489	AOX2	LS
361473	API- 3V	MS
361454	DCI	MS
361494	DCI	LS
361459	FDD	MS
361482	FDD	HS
361483	FDD	MS
361499	FDD	LS
361414	FDD11	HS
361429	FTX	MS
361430	FTX	
361433	FTX	
361457	FTX	MS
361497	FTX	LS
361475	HPD	
361471	ICN	
361426	ID	
361480	ID	HS
361479	II	MS
361476	LSA	MS
361415	TLR	LS
361427	TLR	
361458	TTX	
361477	XOR	MS
361486	XORL	MS

FIGURE 57. MODULES



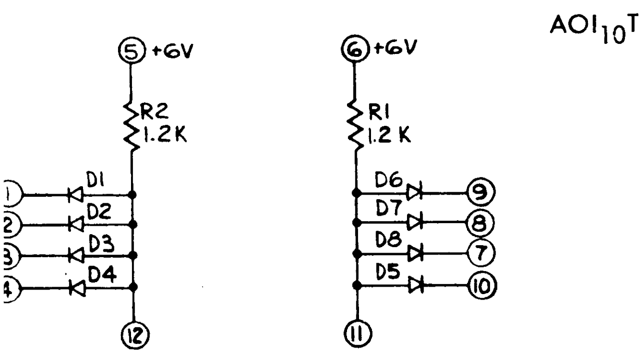
n 361404

igure 58. (AOI10T) AND-OR-Invert-Terminate, High-Speed



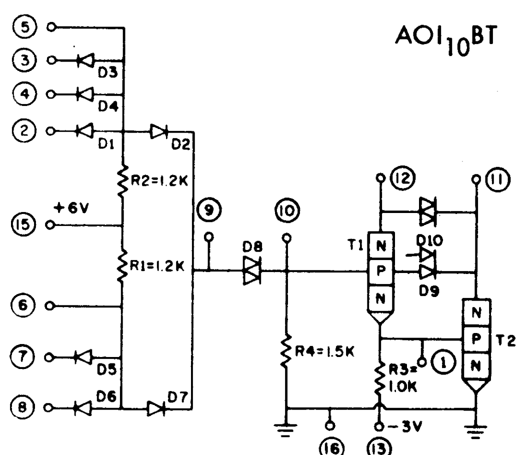
pn 361406

Figure 59. (AOI10B) AND-OR-Invert, High-Speed



n 361405

'igure 60. (AOX10T) AND-OR-Extend-Terminate, High-Speed



pn 361407

Figure 61. (AOI10BT) AND-OR-Invert-Terminate, High-Speed

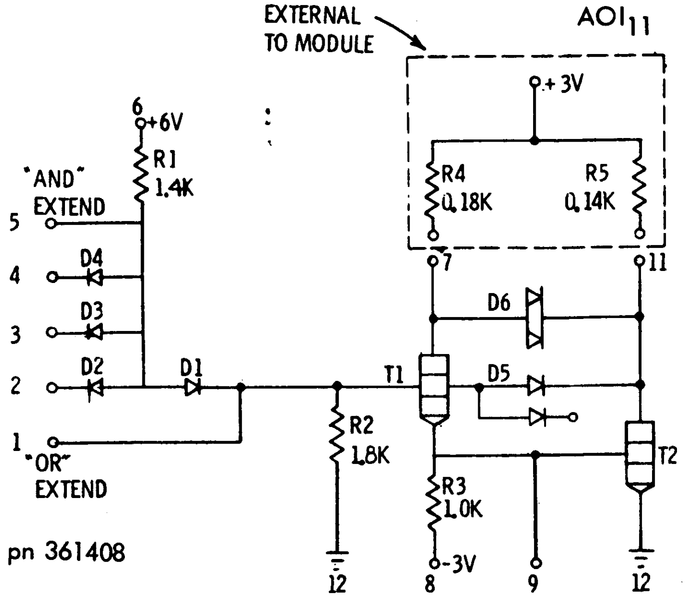


Figure 62. (AOI_{11}) AND-OR-Invert, High-Speed

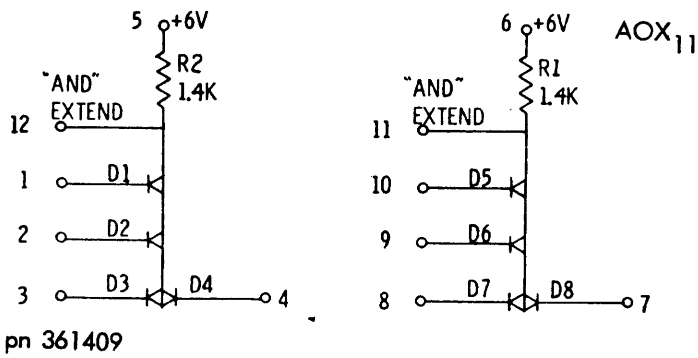


Figure 63. (AOX_{11}) AND-OR-Extend, High-Speed

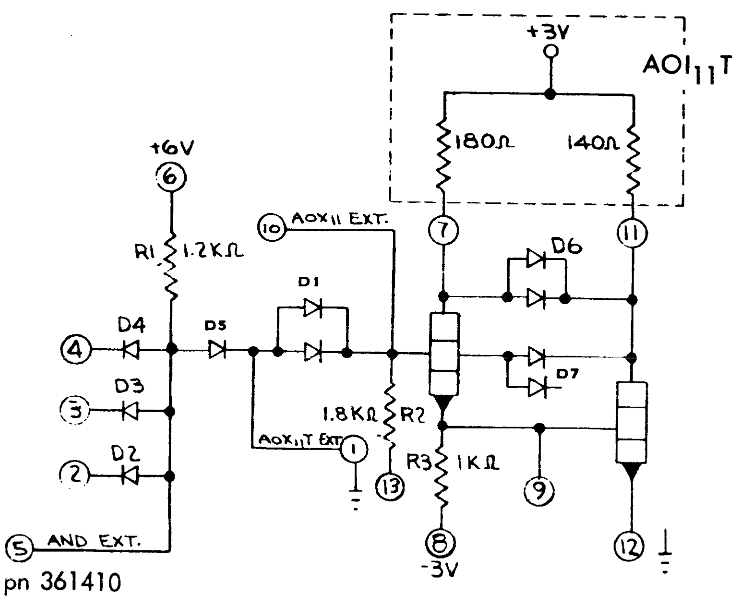


Figure 64. ($AOI_{11}T$) AND-OR-Invert-Terminate, High-Speed

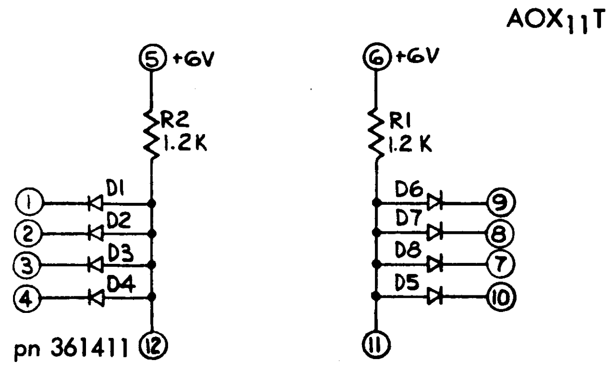


Figure 65. ($AOX_{11}T$) AND-OR-Extend Terminator, High-Speed

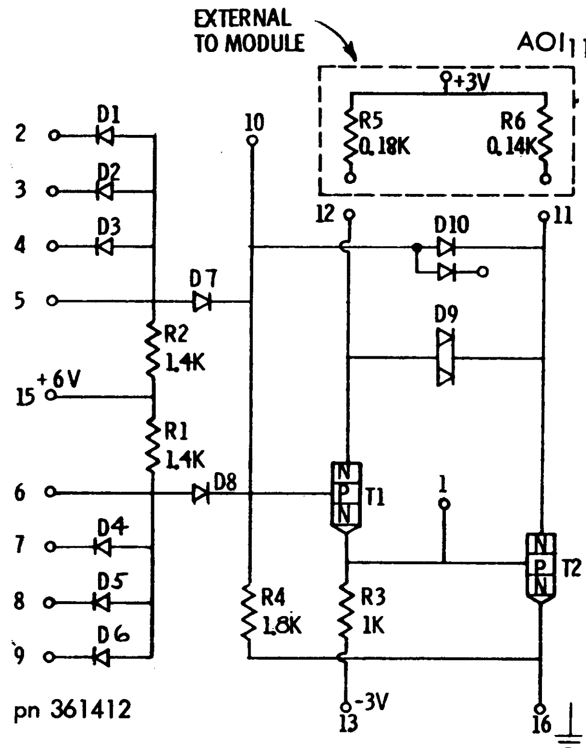


Figure 66. ($AOI_{11}B$) AND-OR-Invert (Two-Way OR), High-Speed

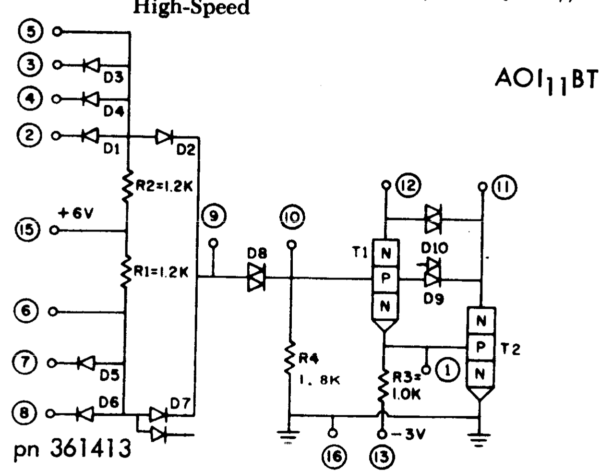
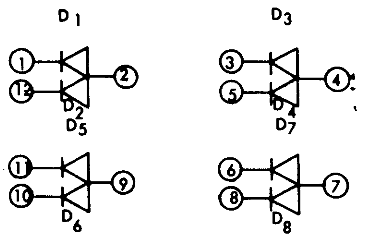


Figure 67. ($AOI_{11}BT$) AND-OR-Invert, High-Speed

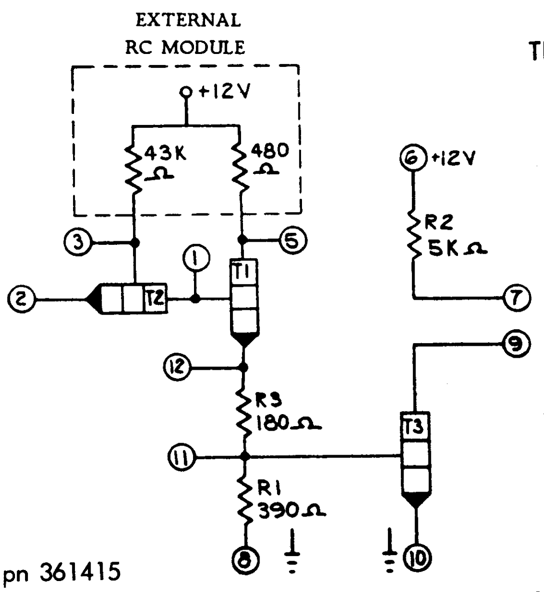
FDD11



pn 361414

Figure 68. (FDD11) Four Double Diodes, High-Speed

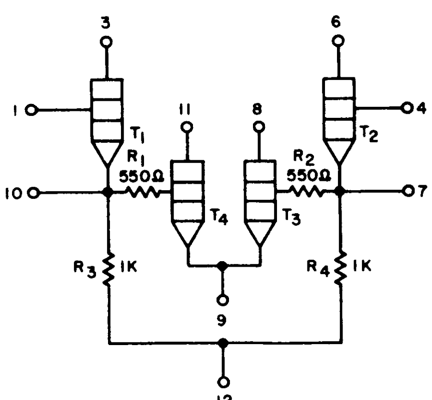
TLR



pn 361415

Figure 69. (TLR) Transmission Line Receiver, Low-Speed

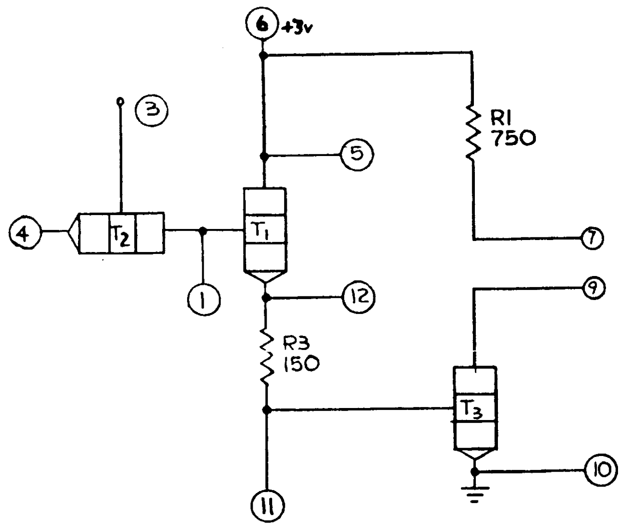
ID



pn 361426

Figure 70. (ID) Indicator Driver, 240 ma

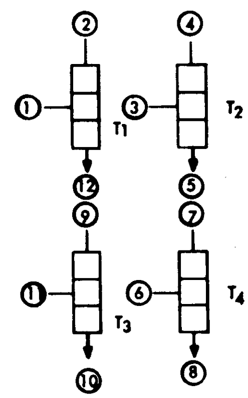
TLR



pn 361427

Figure 71. (TLR) Transmission Line Receiver

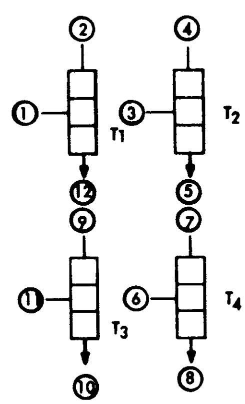
FTX



pn 361429

Figure 72. (FTX) Four Transistors 12v, Medium-Speed

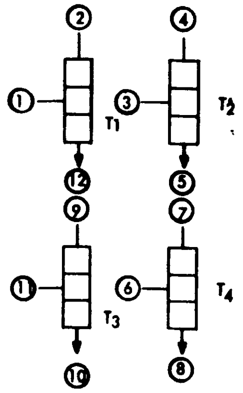
FTX



pn 361430

Figure 73. (FTX) Four Transistors

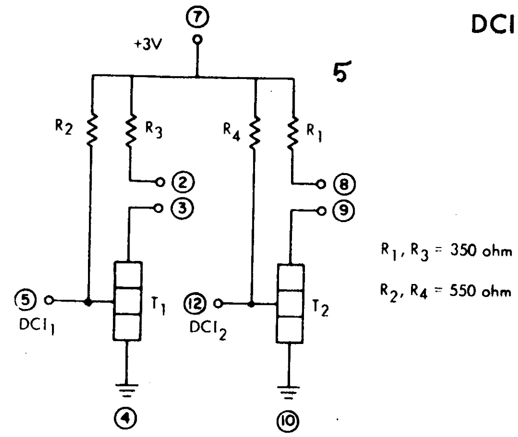
FTX



pn 361433

Figure 74. (FTX) Four Transistors

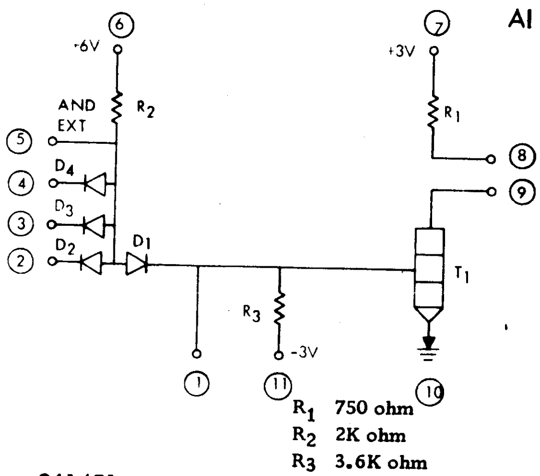
DCI



pn 361454

Figure 77. (DCI) Direct Coupled Inverter, Medium-Speed

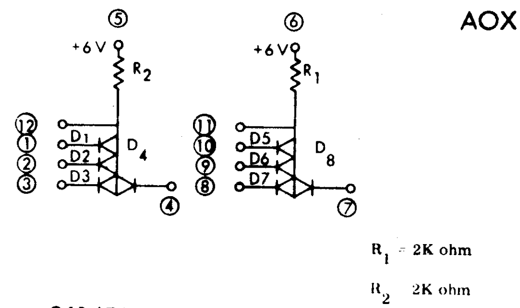
AI



pn 361451

Figure 75. (AI) AND-Invert, Medium-Speed

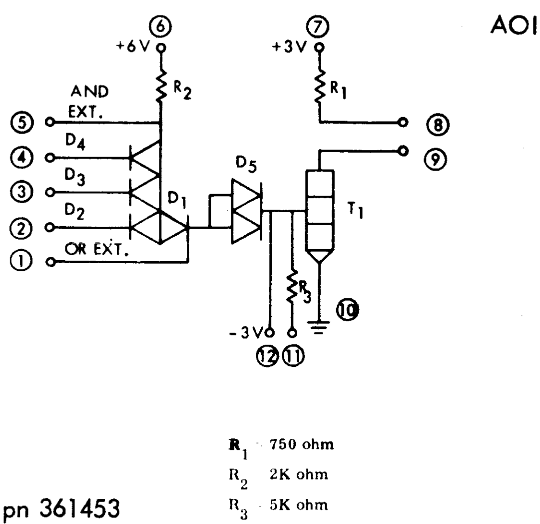
AOX



pn 361455

Figure 78. (AOX) AND-OR-Extender, Medium-Speed

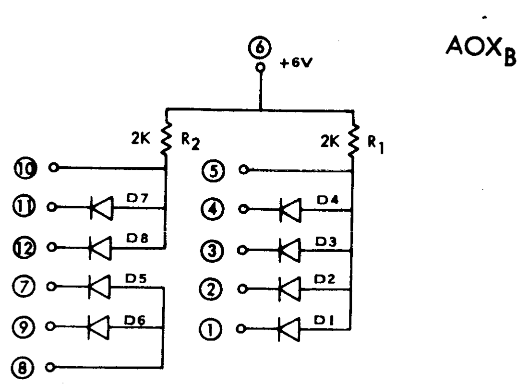
AOI



pn 361453

Figure 76. (AOI) AND-OR-Invert, Medium-Speed

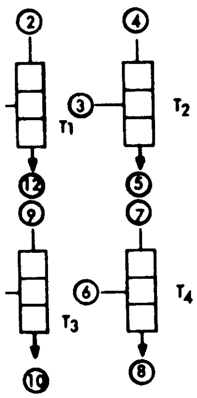
AOX_B



pn 361456

Figure 79. (AOX_B) AND-OR-Extend, Medium-Speed

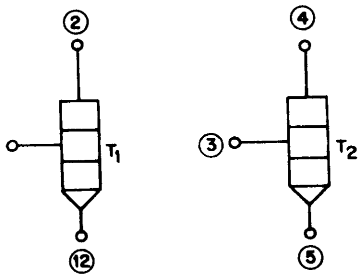
FTX



361457

ure 80. (FTX) Four Transistors 9v, Medium-Speed

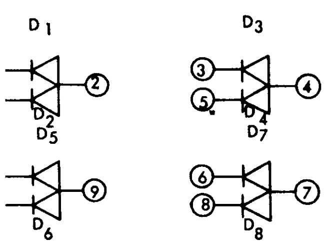
TTX



361458

ure 81. (TTX) Two Transistors, Medium-Speed

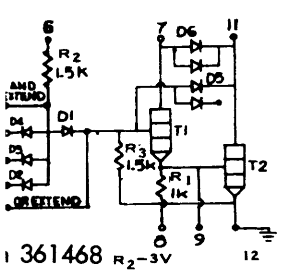
FDD



361459

ure 82. (FDD) Four Double Diodes, Medium-Speed

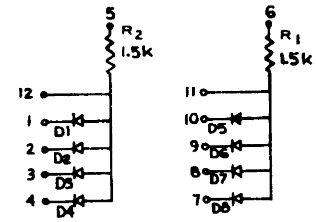
AOI_{10}



361468 R_2-3V

ure 83. (AOI_{10}) AND-OR-Invert, High-Speed

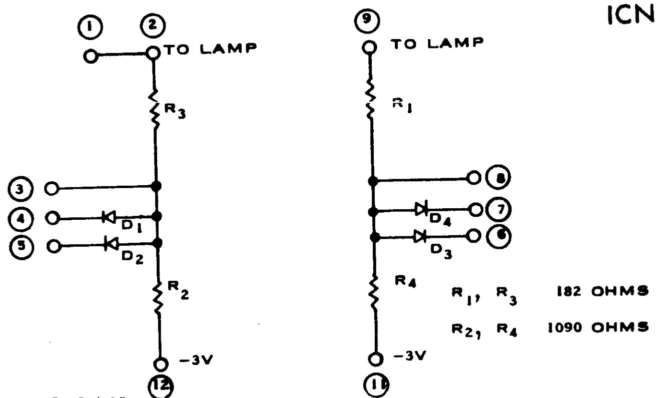
AOX_{10}



pn 361469

Figure 84. (AOX_{10}) AND-OR-Extend, High-Speed

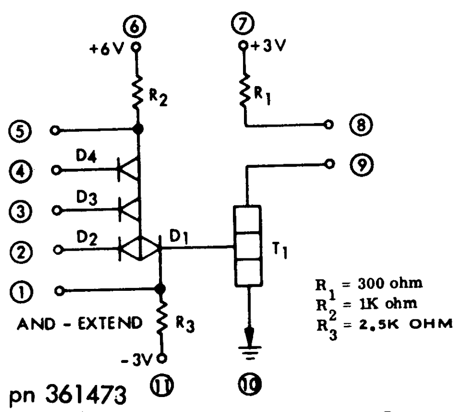
ICN



pn 361471

Figure 85. (ICN) Indicator Coupling Network

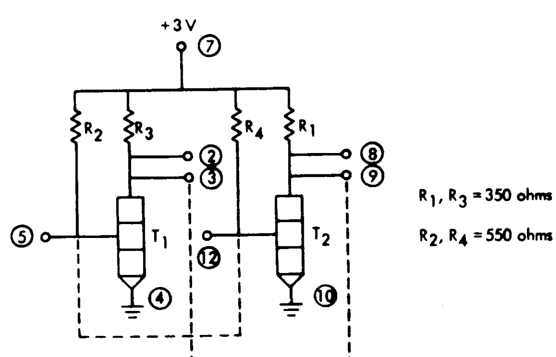
API (3v)



pn 361473

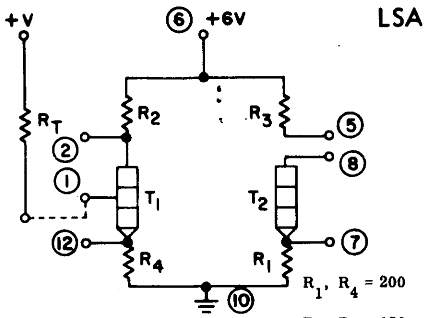
Figure 86. (API) (3v) AND-Power-Inverter, Medium-Speed

HPD



pn 361475

Figure 87. (HPD) High Power Driver



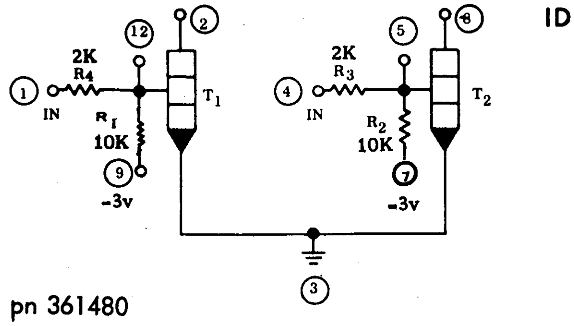
R_1, R_4 = 200

R_2, R_3 = 150

R_T is external to the module.

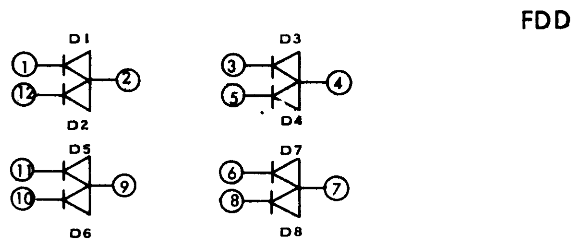
pn 361476

Figure 88. (LSA) Line Sense Amplifier, Medium-Speed



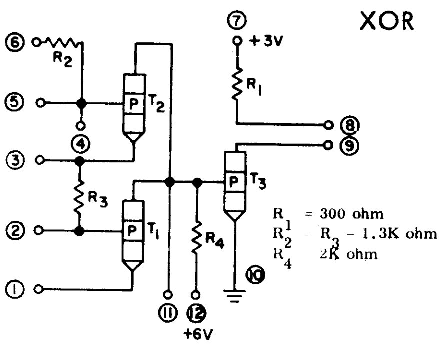
pn 361480

Figure 91. (ID) Indicator Driver, High-Speed



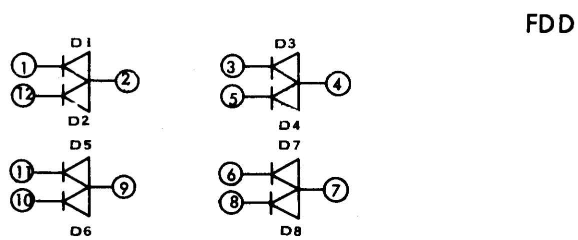
pn 361482

Figure 92. (FDD) Four Double Diodes, High-Speed



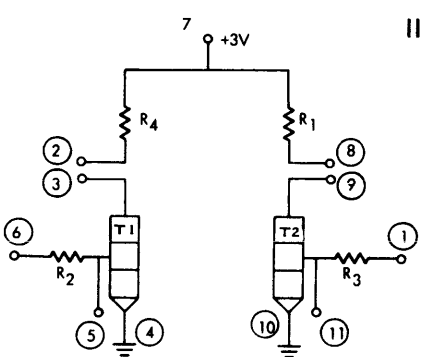
pn 361477

Figure 89. (XOR) Exclusive OR, Medium-Speed



pn 361483

Figure 93. (FDD) Four Double Diodes (General Purpose), Medium-Speed

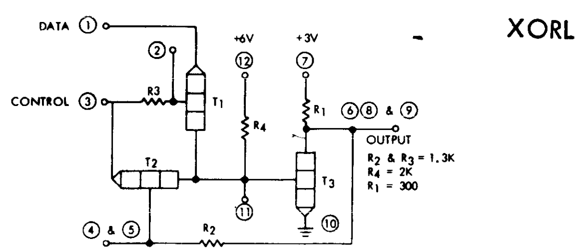


R_1, R_4 · 350 ohms

R_2, R_3 = 1.2K

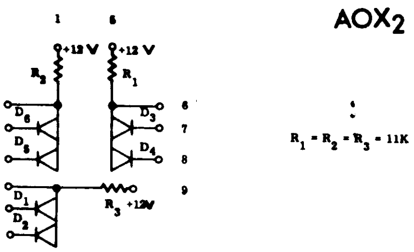
pn 361479

Figure 90. (II) Isolating Inverter, Medium-Speed



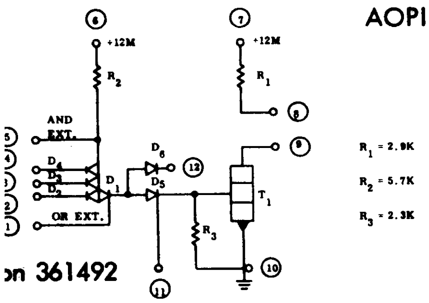
pn 361486

Figure 94. (XORL) Exclusive OR Latch, Medium-Speed



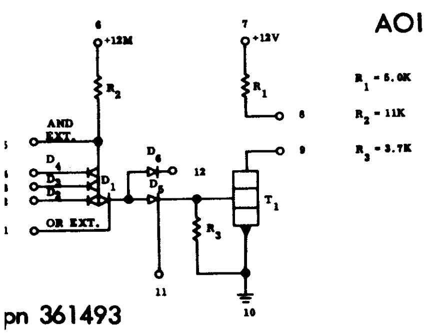
n 361489

igure 95. (AOX$_2$) AND-OR-Extender, Low-Speed



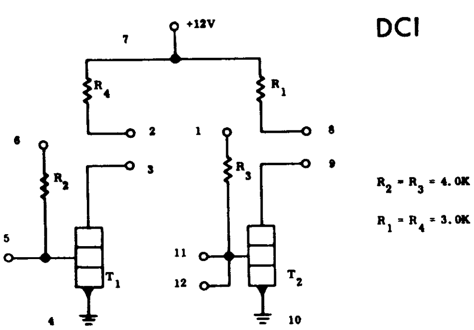
n 361492

igure 96. (AOPI) AND-OR-Power-Inverter, Low-Speed



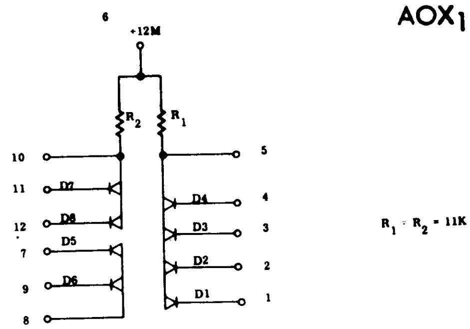
pn 361493

Figure 97. (AOI) AND-OR-Invert, Low-Speed



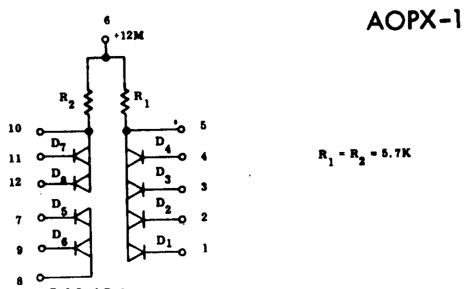
pn 361494

Figure 98. (DCI) Direct Coupled Inverter, Low-Speed



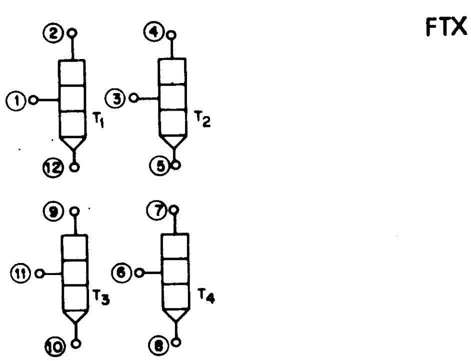
pn 361495

Figure 99. (AOX$_1$) AND-OR-Extender, Low-Speed



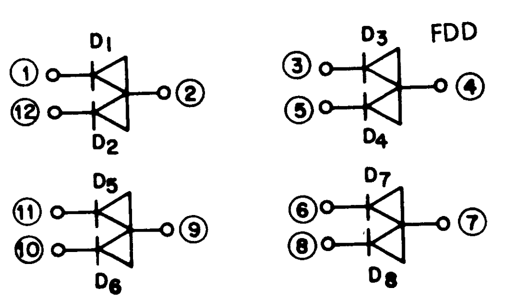
pn 361496

Figure 101. (AOPX$_1$) AND-OR-Power-Extender



pn 361497

Figure 102. (FTX) Four Amplifier and Saturating Transistors, Low-Speed



pn 361499

Figure 103. (FDD) Four Double Diodes

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CIRCUIT CONFIGURATIONS (By Circuit Number)

Figures 107 through 168 in the Reference Section of this handbook are representative examples of circuits (designated by circuit number) actually used on the card layout. The ALD block is included for each circuit. The module pin numbers and connections within the card are represented by the numbers within squares. The card pin numbers are represented by the numbers adjacent to circles.

THE LOAD EQUATION

This equation is applicable to all the basic circuits of the 30 nsec SLT family and provides a means for monitoring the output loading and ensuring against circuit overload. Any circuit not covered by this equation will be described independently.

$$I_{max} \geq C\frac{dv}{dt} + I_{RC} + K_1N_1 + K_2N_2 + K_3N_3 \ldots .$$

where

I_{max} = Maximum current allowable (milliamperes).

I_{RC} = Collector load resistor current.

$C\frac{dv}{dt}$ = Current required for driving worst case capacitance. This factor is stated in the specification for each circuit module.

K_1 = Input load current constant of a driven circuit, e.g., 2.3 ma for the AI's.

N_1 = The number of driven circuits.

K_2 = Input load current constant of a 2nd type of circuit, i.e., 3.0 ma for the AOI's.

N_2 = Number of K_2 input loads.

K_3N_3 etc., until I_{max} is reached.

Sample solution:

For an AI driving 2 AOI's and 2 AI's, the equation solution would be as follows:

I_{max} = 22.5 ma

$C\frac{dv}{dt}$ for AI (Driver) = 3.5 ma

K_1 for AOI = 3.0 ma ($N_1 = 2$)

K_2 for AI = 2.3 ma ($N_2 = 2$)

22.5ma $\geq$ 3.5 + (3.0) (2) + (2.3) (2) ma

22.5ma $\geq$ 3.5 + 6.0 + 4.6 ma

22.5ma $\geq$ 14.1 ma, and the load equation is satisfied.

CONDENSED CIRCUIT SPECIFICATIONS

This section contains circuit specifications only for those circuits considered to be basic building blocks. These specifications are abbreviated to include only that information required for machine design.

AND-INVERT MEDIUM SPEED (AI) - 361451

The AI module (Figure 75) consists of a diode positive AND circuit followed by a saturating transistor inverter.

Input Requirements

a. K = AI input load current constant = 2.3 ma.

b. Maximum of 5 AND diodes (considering specified worst-case delay).

c. Maximum of 64 AND diodes allowable (neglecting specified worst-case delay).

d. Maximum of 19 AND diodes can be switched simultaneously (neglecting specified worst-case delay).

e. All extended AND diodes to be on the same small card as the AI module. (This limitation is necessary to minimize stray capacitance and junction temperature differences between the extended AND diodes and the translate diode of the AI module.

Load Equation

$$22.4 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + \ldots\ldots$$

$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

DOT OR'd Collectors

DOT OR'ing will be limited to 5 collectors.

The distance between DOT OR'd blocks is limited only when one of the DOT collectors must remain on when the other collectors are turned off. The distance between AI loads and any collector remaining on is limited to a maximum of ten inches of line.

Application Notes

Wiring Rules; Input and Output Restrictions and Criteria

a. Maximum Net Length. The maximum net length at either the input or the output should not exceed 6 feet of line. This restriction is required to prevent excessively long circuit delays.

b. Input Restrictions. With a single wire in a channel, the input line to an AI must not exceed 3 feet if driven by an AI or AOI. It must not exceed 2 if driven by an API or 1.5 feet if driven by a DCI. If there are two other lines in the channel switching simultaneously, the maximum length is 18 inches. These restrictions are required because of reflections and noise coupling, respectively.

c. Output Restrictions. Caution must be exercised in the use of DOT collectors since simultaneous noise pulses can exist at the base of each paralleled transistor.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_2	10.5	12.8	11.9	14.7
R_3	4.37	2.95	4.6	3.5
R_1	11.0	0	11.8	0
D_1	1.02	0.28	1.38	0.62
$D_2D_3D_4$	0	1.49	0	1.28
T_1	5.18	0	5.07	0
Total Power Dissipated	32.17	17.52	34.75	20.10

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Power Requirements

The voltage tolerange (for WC EOL) is ±4% at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+6vM	+2.3	+2.6	+2.5	+2.78
+3v	+3.84	+0	+4.06	+0
-3v	-1.09	-0.93	-1.16	-1.01
GND	-16.25	-0	-17.05	-0
Sign Convention:	+ Current out of supply - Current into supply			

AND - OR - INVERT (AOI) - 361453

The AOI module (Figure 76) consists of a diode positive AND function and one diode for an OR function, followed by a saturating transistor inverter. The fan-in to the AND is accomplished by connection to the common anode diodes from the FDD module. A pin is available for extending the fan-in to the OR by connection to an OR diode from the AOX module. Extension is accomplished by connecting the pins on the small card, for most applications. For DOT collectors, only one collector resistor is required for the common collector connection. If more collector resistors are connected, the fan-out is reduced accordingly.

Input Requirements

a. K = AOI input load current constant = 3.0 ma.

AND Fan-In Rules

Limitations on number of AND diodes;

a. Maximum of 5 (considering specified worst-case delays.

b. Maximum of 19 AND diodes can be switched simultaneously (neglecting specified worst-case delay).

c. Maximum of 64 AND diodes allowable (neglecting specified worst-case delay).

d. All extended AND diodes should be on the same small card as the AOI module. (This limitation is necessary to minimize stray capacitance and junction temperature differences between the extended AND diodes and the translate diode of the AOI module.)

OR Fan-In Rules

a. Maximum of 5 OR inputs.

b. All extended OR diodes to be on the same small card as the AOI module to minimize stray capacitance and large temperature differences between diode junctions.

c. OR input signals are simultaneous when the skew between any two switching OR inputs is 90 nanoseconds or less.

d. The worst-case T_{OFF} delay increases approximately 7 nanoseconds for each additional OR input.

Load Equation

$$22.5 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + \ldots.$$

$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

DOT OR'd Collectors

DOT OR'ing will be limited to 5 collectors.

The distance between DOT-OR'd blocks is limited when one of the DOT collectors must remain on when the other collectors are turned off. The distance from the load to any collector remaining on is limited to a maximum of 10 inches of line.

a. Maximum Net Length. The maximum net length at either the input or the output should not exceed 6 feet of line. This restriction is required to prevent excessively long circuit delays.

b. Input Restrictions. With a single wire in a channel, the input line to an AOI must not exceed five feet if driven by an AI or AOI. It must not exceed three feet if driven by an API or DCI. If there are two other lines in the channel switching simultaneously, the maximum length is 30 inches. These restrictions are necessary to limit reflections and noise coupling.

c. Output Restrictions. Caution must be exercised in the use of DOT collectors since simultaneous noise pulses can exist at the base of each paralleled transistor.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_2	8.0	13.0	9.0	15.0
R_3	4.0	2.0	4.0	2.0
D_1D_5	4.0	2.0	4.0	2.0
$D_2D_3D_4$	0	2.0	0	2.0
R_1	11.0	0	12.0	0
T_1	7.0	0	8.0	0
Total Power Dissipated	34.0	19.0	37.0	21.0

Power Requirements

The voltage tolerance (for WC EOL) is ±4% at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+5vM	+2.00	+2.5	+2.1	+2.8
+3v	+3.7	+0	+4.1	+0
-3v	-0.8	-0.6	-0.9	-0.7
GND	-20.3	0	-25	0
Sign Convention:	+ Current out of supply			
	- Current into supply			

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

DIRECT COUPLED INVERTER (DCI) - 361454

The DCI module (Figure 77) contains two separate direct-coupled inverters. The inverters were designed to provide a fast, economical way of extending the fan-out of an AI or an AOI module by a factor of 2.26. The lead length between the outputs of the AI, or AOI, and the DCI must be minimized if the full speed capability of this circuit is to be realized.

The two DCI's of the module were not designed for parallel operation. For higher fan-out, the High Power Driver (HPD) should be used.

Input Requirements

a. The DCI must be driven by a loaded AI or AOI. The AI or AOI must not drive any additional load.

b. Input $\geq$ 2.1 ma for specified collector current of 51 ma. The I_b on minimum for T_1 or T_2 is 5 ma; 2.9 ma is provided by each of the 550-ohm resistors to the +3v supply.

Load Equation

$$51 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 \ldots.$$

$$C \frac{dv}{dt} = 5 \text{ ma (for } C = 110 \text{ pf)}$$

The DCI may drive 15 AI's, 15 AOI's, or 7 API's.

Application Notes

a. Maximum Net Length. The maximum net length at output should be less than 6 feet. This is required to prevent excessively long circuit delay.

b. Input Restrictions. The input line length is restricted to 6 inches because of coupled noise when adjacent lines are switching. The block driving the DCI cannot have additional fan-outs.

c. Output Restrictions. The maximum single wire length should be less than 1.5 feet to limit reflections and coupled noise.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_2 or R_4	9	14	10	17
R_1 or R_3	22	0	25	0
T_1 or T_2	22	0	24	9
Total Single DCI Power Dissipation	53	14	59	17
Total Maximum Power Dissipation on the Module	106	28	118	34

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Power Requirements

The voltage tolerance (for WC EOL) is ±4% at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+6vM	-	-	-	-
+3v	+12	+5	+13	+6
-3v	-	-	-	-
GND	-58	0	-59	0
Sign Convention:	+ Current out of a supply.			
	- Current into a supply.			

AND POWER INVERTER (API 3V) - 361473

The API module (Figure 86) is used as a power inverter with logic capability at the input. The API serves the same logic function as the AI module, but has a higher fan-out capability. The API module consists of a diode positive AND circuit followed by a saturating inverter.

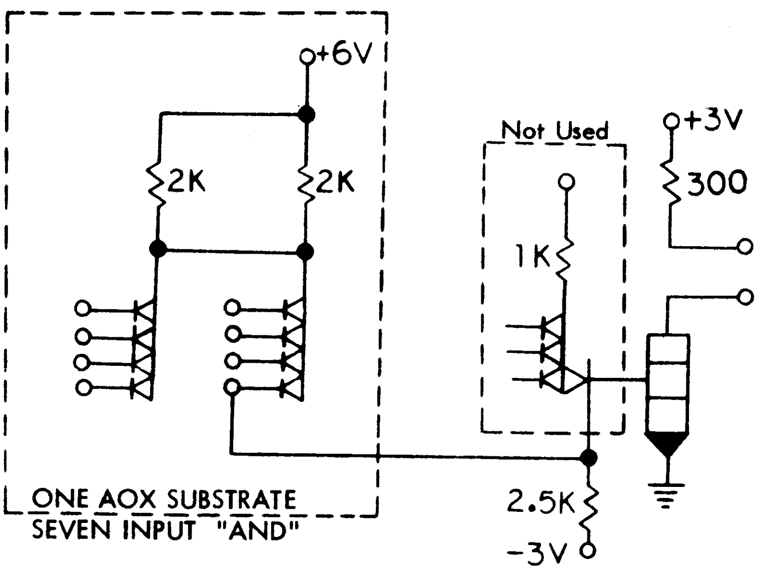
Input Requirements

a. K = API input load current constant = 5.0 ma.

b. Maximum of 5 AND diodes (considering specified worst-case delay).

c. Maximum of 7 AND diodes allowable (neglecting specified worst-case delay).

Extension of the AND can be made by using an AOX substrate only on the same first level package as the API, in the manner shown below.



Note: The 1K Resistor must not be returned to a Power Supply

Load Equation

$$38 \text{ ma} \geq C\frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + N_3K_3 \ldots.$$

$$C\frac{dv}{dt} = 4 \text{ ma}$$

DOT OR'd Collectors

DOT OR'ing will be limited to five collectors.

The distance between DOT OR'd blocks is limited only when one of the dotted collectors must remain on when the other collectors are turned off.

The distance of API loads to any collector remaining on is limited to a maximum of six inches of line.

The API can drive 4 API's, 10 AI's, 1 DCI, or 1 HPD.

Application Notes

Wiring Rules: Input and Output Restrictions and Criteria

a. Maximum Net Length. The maximum net length at either the input or the output must not exceed 6 feet of line. This restriction is required to prevent excessively long circuit delays.

b. Input Restrictions. The input line to an API must not exceed 4 feet if driven by an API or a DCI. This is for a single wire in a channel. If there are two other lines in a channel switching simultaneously, the maximum input line length is 18 inches. These restrictions are necessary to limit reflections and noise coupling.

c. Output Restrictions. Caution must be exercised in the use of DOT collectors since simultaneous noise pulses can exist at the base of each parallel transistor.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_1	28	0	29	0
R_2	19	26	20	29
R_3	6	5	7	5
D_1	3	1	4	1
$D_2D_3D_4$	0	3	0	0
T_1	11	0	13	0
Total Power Dissipated	67	35	73	38

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Power Requirements

The voltage tolerance (for WC EOL) is ±4% at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+6vM	+ 4.4	+5.2	+ 4.6	+5.5
+3v	+ 9.2	0	+10.1	0
-3v	- 1.6	-1.3	- 1.8	-1.5
GND	-32.3	0	-35.3	0
Sign Conventions:		+ Current out of a supply. - Current into a supply.		

HIGH POWER DRIVER (HPD) - 361475

The HPD module (Figure 87) is a specially selected DCI module with the two inverters wired in parallel. The driving block can be an AI or AOI, but the collector resistor has to return to a +6v supply. An API can also be used to drive the HPD. The HPD has a fan-out capability of 36 AI's, or equivalent, load.

Input Current Requirements

$I_{in} \geq 5.8$ ma for specified collector current of 111 ma.

The I_b on minimum for T_1 and T_2 is 11.6 ma; 5.8 ma is provided by each of the 550-ohm resistors to the +3v supply.

Input Restrictions

The driving block must be on the same small card and adjacent to the HPD. The maximum wire length between the driver and the HPD must not exceed one inch.

Load Equation

$$111 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + N_3K_3 \; \ldots .$$

$$C \frac{dv}{dt} = 10 \text{ ma (for 220 pf)}$$

Application Notes

Wiring Rules: Input and Output Restrictions and Criteria

a. Maximum single line length is six inches when only one load is being driven at the end of the line. No maximum load restriction.

b. A minimum of at least three AI loads, or equivalent, must be at the end of the line if it is one foot long. This is necessary to prevent large reflections. The maximum load on each one foot line is 12 AI's or equivalent.

c. For single line length longer than one foot and extending to another mother board, the line must be terminated. The maximum single line length is four feet and the maximum loading is six AI's per line or equivalent.

d. The maximum net length in this case can be as much as 24 feet, but the delays specified in the Circuit Flyer are for a worst-case net length of six feet.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_1	22	0	25	0
R_3	22	0	25	0
R_2	9	14	10	17
R_4	9	14	10	17
T_1	23	0	25	0
T_2	23	0	25	0
Total Power Dissipation	108	28	120	34

NOTE: When load sharing between T_1 and T_2 is not equal, one transistor may dissipate as much as 70% of the total transistor power dissipation.

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Power Requirements

The voltage tolerance (for WC EOL) is $\pm 4\%$ at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal		Maximum	
	ON	OFF	ON	OFF
+6vM	-	-	-	-
+3v	23	5	26	6
-3v	-	-	-	-
GND	-125	0	-126	0
Sign Convention: + Current out of a supply. - Current into a supply.				

ISOLATING INVERTER (II) - 361479

The II module (Figure 90) contains two separate inverters. Each inverter presents a 1.2K series resistance when connected to the driving block.

Input Current Requirements

a. $K = I_{dc}$

b. I_{dc} = Steady state d-c input current = -0.9 ma (Up-level load only).

c. No more than one II to be driven by any AI or AOI.

d. No more than two II's to be driven by any API.

Load Equation

$$27 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + \ldots$$

$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

$$I_{RC} = 8.7 \text{ ma}$$

Application Notes

Wiring Rules: Input and Output Restrictions and Criteria.

a. Maximum Net Length. The maximum net length at either input or output should not exceed six feet of line. This is necessary to prevent excessively long circuit delays.

b. Input Restrictions. The input line length should not exceed nine inches to prevent excessive coupled noise.

c. Output Restrictions. The maximum single wire length should be less than 1.5 feet to limit large reflections and coupled noise.

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_1 or R_4	21	0	25	0
R_2 or R_3	1.4	0	1.8	0
T_1 or T_2	8.0	0	8.5	0
Total Power Dissipation	30.4	0	35.3	0

Overvoltage Requirements to Prevent Component Damage

Power Supply	V_{max}
+6v	+9v
+3v	+8v
-3v	-8v

Any significant overvoltage condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Marginal Check

Does not apply for this circuit.

Power Requirements

The voltage tolerance (for WC EOL) is $\pm$4% at the small card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+6vM	-	-	-	-
+3v	7.7	0	8.8	0
-3v	-	-	-	-
GND	-23.8	0	-25.1	0

Sign Convention: + Current is out of supply.
- Current is into a supply.

15 MA SWITCH (ID) - 361480

The ID module (Figure 91) contains two indicator driver circuits.

Input Requirements

I_{in} = 0.97 ma (Up-level load only).

Load Equation

Does not apply.

Output Specifications

I_c max = 19.0 ma at V_{CE} = 0.30v

Application Notes

High-Speed ID Application (Using Lamp Number 2-456-OL6 in collector circuit and +3v Power Supply).

Wiring Rules. The wire length from the output of the ID to the lamp can include all of the following lengths:

a. 10 feet of large card wiring.

b. 30 feet of flat cable.

c. 180 feet of No. 22 wire.

The wire length from the output of the driving AOI-10T or AOI-10 to the indicator should be kept to a minimum since this length must be included as part of the total net length drive.

Medium-Speed Application (Using Lamp Number 2-456-OL6 in collector circuit and +3v Power Supply).

Wiring Rules. The wire length from the output of the ID to the lamp can include the following lengths:

a. 10 feet of large card wiring.

b. 50 feet of flat cable.

Component Power Dissipation in Milliwatts

Component	Maximum Value (mw)	
	ON	OFF
$R_3 = R_4$	2.30	0
$T_1 = T_2$	9.44	0
Circuit Total	11.74	0
Module Total	23.48	0

Marginal Check

Not applicable.

Power Requirements

The voltage tolerance (for WC EOL) is ±4% at the small card pins.

Power Supply Current Requirements (as a High-Speed ID). (Two circuits/module.)

Power Supply	Maximum (ma)	
	ON	OFF
GND	32.20	-
-3v	1.14	0.80
Sign Convention:	+ Current out of supply.	
	- Current into supply.	

LINE DRIVER AND TERMINATOR RULES

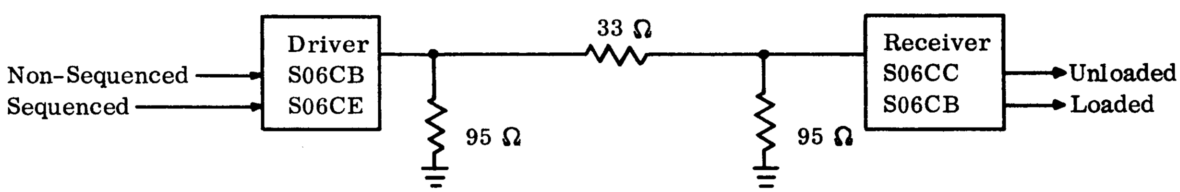
These rules apply to the following circuit cards:

5801664-6	Sequenced-Multiplex-Line Drivers
5808045-6	Multiplex-Line Drivers
5808033-10	Multiplex-Receivers
5800549-10	90-ohm Multiplex Resistor

or any line configuration using the following modules:

S06CB or S06CE	Drivers
S06CC, S06CF	Receivers
S61IG	Terminating Resistors

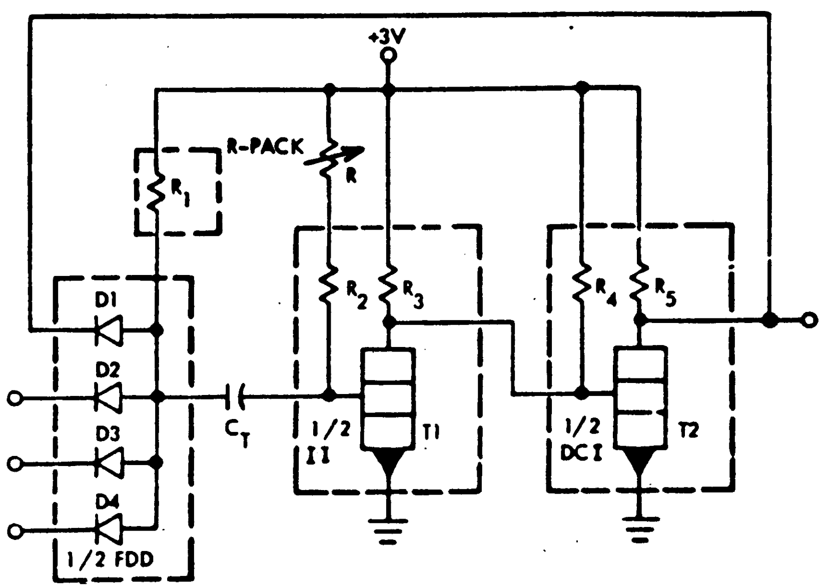
Any combination of the above driver and receiver circuits will be subject to the following rules:



1. The series resistance of any driven line will not exceed 33 ohms, as measured from the output of the driver to the extreme end of the line.
2. A maximum of 14 drivers and 8 receivers, or 8 drivers and 14 receivers on a line.
3. The maximum number of circuits on any one line will not exceed 22.
4. The receivers must not be less than 3 feet apart.
5. No receiver may be located 6 inches beyond the termination of any line.
6. The line must be terminated at both ends with 95 ohms $\pm 1\%$ (parallel equivalent = 47.5 ohms).

SINGLE-SHOT SSB (VARIABLE)

The SSB below uses one-half of an II Module, one-half of a DCI Module, one-half of an FDD Module, a Trim Potentiometer, an R-Pack and Timing Capacitors. The output pulse width is controlled by the 2K Trim Potentiometer and the Timing Capacitor, C_T. For a given C_T, the range of the output pulse width is fixed, and by means of the Trim Potentiometer, a continuous variation can be obtained.



R_1 = 200 Ω
R_2 = 1.2K Ω
R = 25 Ω Trim Potentiometer
R_3 = 350 Ω
R_4 = 550 Ω
R_5 = 350 Ω
C_T = Timing Capacitor

The SSB is triggered by a negative-going pulse, having a transition no greater than 50 nanoseconds and a width no less than 30 nanoseconds. Upon triggering, the output drops to saturation level for the pre-set duration before returning to the +3v level. A minimum recovery time for the capacitor is required before the next trigger pulse can be applied. If the SSB is triggered during the recovery period of the capacitor, the output pulse width will be of incorrect duration. This circuit only uses the +3v supply and is thus free from the marginal check required by the SSA circuit.

Input Current Requirements

$I_{in} = I_{dc} + I_{tr}$ = 7.5 ma = K
I_{dc} = Steady state input current = 5.6 ma
I_{tr} = Transient current = 1.9 ma

NOTE: The current through D_1 also equals 7.5 ma when both the input and output levels are at +0.3v.

AND Fan-In Rules

Maximum of three AND diodes available from one-half of an FDD Module on the same small card (considering specified worst-case delay).

Input Restrictions

The input line is restricted to 1 foot or less to prevent large reflections.

Load Equation

$$36 \text{ ma} \geq C \frac{dv}{dt} + I_{RC} + N_1K_1 + N_2K_2 + \ldots\ldots$$

$$C \frac{dv}{dt} = 5 \text{ ma}$$

$$I_{RC} = 8.5 \text{ ma}$$

Output Restrictions. The maximum single wire length should not exceed 1 foot to prevent excessive reflection and coupled noise when adjacent lines are switching.

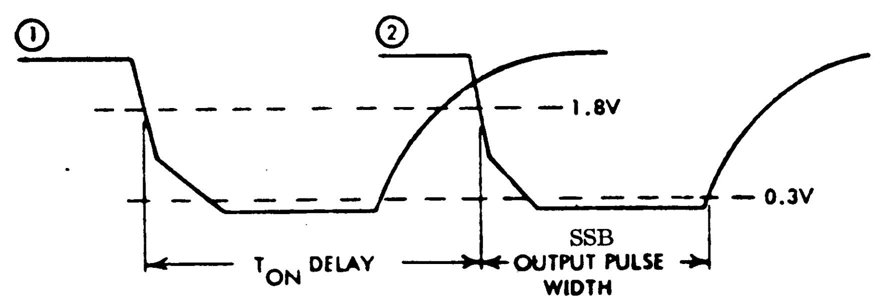
Maximum Net Length. The maximum net length at output should not exceed 6 feet of line. This restriction is required to prevent excessively long circuit delay.

A-C Performance

All delay measurements are taken between input and output of the circuit for input transition of 50 nsec.

Worst-case T_{ON} delay $\leq$ 60 nsec T_{OFF} delay = SBB output pulse width

The T_{ON} delay and SSB output pulse width are defined in the following figure:



Waveform 1 is the input to the SSB
Waveform 2 is the output of the SSB

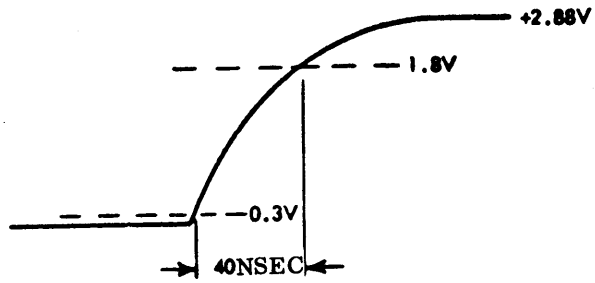
Turn-on Transitions

The turn-on transition time is specified as

$$5 \text{ nsec} \le Tr_{ON} \le 50 \text{ nsec}$$

The typical turn-on transition time is approximately 15 nsec.

The SSB worst-case Tr_{OFF} output is shown in the following figure:



Output Pulse Width and Recovery Time

Definition of Terms

For a given value of C_T, the timing capacitor,

Output Pulse Width Tolerances and Drifts

a. Initial drift with supply tolerances and temperature is -8% and +15%, respectively.

b. Maximum EOL tolerances should be between -25% and +30%.

Recovery Time Tolerances and Drifts

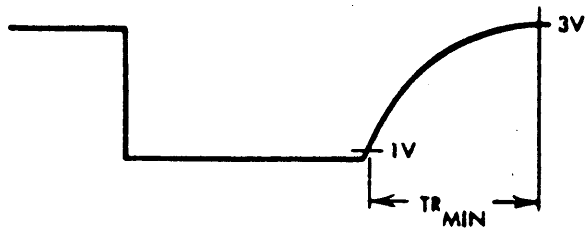
a. Initial drift with supply tolerances and temperature is within ±10%.

T_{max} = Maximum output pulse width (when trim potentiometer is at maximum resistance)

T_{min} = Minimum output pulse width (when trim potentiometer is at minimum resistance)

TR_{min} = Minimum recovery time required for capacitor C_T.

The output pulse width is measured between +1.8v and +0.3v. The recovery time TR_{min} is measured at the common anode point of the diodes, and the levels are +1.0v and +3.0v. The waveform of the common anode of the input diodes is shown in the following figure:



Output Pulse Width and Recovery Time

C_T		T_{max}		T_{min}		TR_{min}	
100	pf	207	nsec	78	nsec	92	nsec
300	pf	620	nsec	234	nsec	276	nsec
0.001	uf	2.07	usec	780	nsec	920	nsec
0.0033	uf	6.85	usec	2.57	usec	3.04	usec
0.01	uf	20.7	usec	7.8	usec	9.2	usec
0.033	uf	68.5	usec	25.7	usec	30.4	usec
0.1	uf	207	usec	78	usec	92	usec
0.33	uf	685	usec	257	usec	304	usec
1.0	uf	2.07	msec	780	usec	920	usec
3.3	uf	6.85	msec	2.57	msec	3.04	msec
10	uf	20.7	msec	7.8	msec	9.2	msec
27	uf	56.0	msec	21.0	msec	25	msec
Above values based on nominal component values.							

$T_{max} = 2.07 \times 10^3\ C_T$ seconds

$T_{min} = 0.78 \times 10^3\ C_T$ seconds

$TR_{min} = 0.92 \times 10^3\ C_T$ seconds (C_T has units of farads)

Power Requirements:

The voltage tolerance (for WC EOL) is ±4% at the same card pins.

Power Supply Current Requirements in Milliamperes

Power Supply	Nominal (ma)		Maximum (ma)	
	ON	OFF	ON	OFF
+6vM	-	-	-	-
+3v	+29.9	+14.8	+32.7	+15.9
-3v	-	-	-	-
GND	-56.4	-14.8	-59.2	-15.0
Sign Convention:	+ Current out of a supply. - Current into a supply.			

Component Power Dissipation in Milliwatts

Component	Nominal (mw)		Maximum (mw)	
	ON	OFF	ON	OFF
R_1	20	0	24	0
R_2	7	2	8	2
R (Trim Pot)	7	2	8	2
R_3	9	21	11	24
R_4	6	13	7	15
R_5	21	0	24	0
D_1	13	0	13	0
D_2, D_3, D_4	6	0	6	0
T_1	0	5	0	5
T_2	25	0	26	0
Total Power Dissipation	114	43	127	48

Undervoltage and Overvoltage Requirements

Steady State Requirements

Power Supply	V_{min} (Undervoltage)	V_{max} (Overvoltage)
+6v	+4.5v	+9v
+3v	0v	+4.2v
-3v	0v	-5.25v

Transient Requirements

Power Supply	V_{min} (Undervoltage)	V_{max} (Overvoltage)
+6v	0v	+9v
+3v	0v	+8v
-3v	0v	-8v

Any significant transient condition should not exceed 50 milliseconds.

Power Sequencing

None required for this circuit.

Marginal Checking

Not applicable for this circuit.

POWER DISTRIBUTION

(From Specification # 811800)

VOLTAGE TOLERANCES

Power Supply Tolerances

Power supplies for the 5 and 30 nanosecond circuit families must regulate to within ±2% of the nominal value.

Power supplies for the 700 nanosecond circuit family must regulate to within ±5% of the nominal value.

The power supply tolerances include dynamic line changes, dynamic load changes, ripple and thermal drift, and are to be determined by measuring at the supply terminals.

When remote sensing is necessary, such remote sensing point will be defined at or near the lateral center of the distribution plane, which is that area at the logic gate or frame that is serviced by a group of power supplies supplying power to the same group of boards and sharing the same ground return path. Conductors assigned solely to the sense function should be routed from the supplies to the designated sense point.

Standard voltages for SLT applications are +3v, -3v, and +6v for the 5 and 30 nanosecond circuit families, and +12v and +12M for the 700 nanosecond circuit family.

Distribution System Tolerances

The distribution system shall be responsible for not more than 2% variation from the normal voltages. The tolerance is measured at the card socket. The d-c ground shift is measured from the input to the laminar bus, to the card socket. Ground and voltage transients are held to specified values by card decoupling.

To establish a distribution system that will meet the requirements as set forth in this manual, values of load current for a given supply voltage were determined from several representative machines. Each six-pack socket location was assigned the same value of load currents and a uniformly distributed load condition was assumed.

Power supply, distribution system, and transient noise tolerances for the various circuit families are given in the table below and in Figure 104.

Family : (Nanoseconds)	Voltage to Ground* (On Board)	Voltage to Ground** (On Card)
5-10	a. A_1 = 100 mv; t_1 = 30 nsec b. A_2 = 200 mv; t_2 = 15 nsec	a. A_1 = 250 mv; t_1 = 30 nsec b. A_2 = 500 mv; t_2 = 15 nsec
30	a. A_1 = 100 mv; t_1 = 40 nsec b. A_2 = 200 mv; t_2 = 20 nsec	a. A_1 = 250 mv; t_2 = 40 nsec b. A_2 = 500 mv; t_2 = 20 nsec
700	a. A_1 = 250 mv; t_1 = 100 nsec b. A_2 = 500 mv; t_2 = 50 nsec	a. A_1 = 500 mv; t_1 = 100 nsec b. A_2 = 1 volt; t_2 = 50 nsec

* Measured from a voltage pin to the ground pin within the same six-pack socket location; not to exceed the limits A_1 and t_1 or A_2 and t_2.

**Measured from a voltage pin of a module to the board ground pin within the same six-pack socket location; not to exceed the limits A_1 and t_1 or A_2 and t_2.

A combined a-c and d-c ground shift between any two points within a page or gate in any circuit family shall not exceed 100 millivolts.

The combined a-c and d-c ground shift between the ground pin of any module and the board ground pin within the same six-pack socket location shall not exceed:

a. 100 mv 5-10 nsec family

b. 100 mv 30 nsec family

c. 200 mv 700 nsec family

Noise will be kept within the limits stated.

All voltage distribution media are rated for 90 volts d.c., and are capable of withstanding 900 volts rms for one minute, without breakdown.

For applications of 0 - 90 volts d.c.: Ten times the rated voltage but not less than 100 volts rms.

For applications higher than 90 volts: The test voltage is three times the rated voltage but not less than 900 volts rms.

The voltage distribution system does not provide for the integration of 700 nanosecond family circuits with faster circuit families within the same board.

When 700 nanosecond family circuits are integrated with faster circuits within the same gate, the different families of circuits shall be located so that voltage distribution for both is practical.

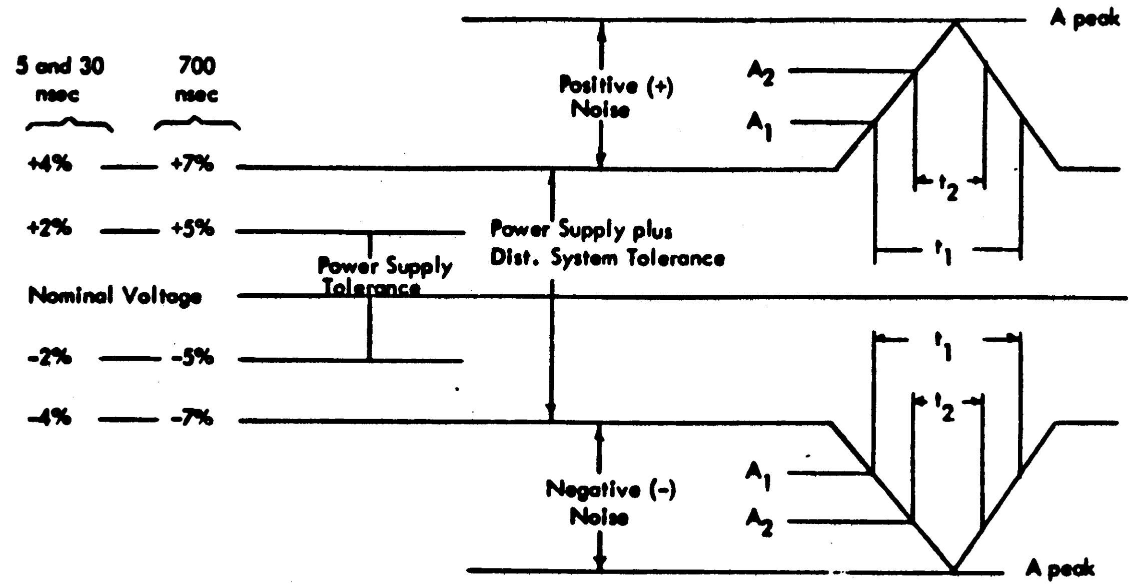


Figure 104. Power Supply Noise

MINI-BUS

Description

The MINI-BUS consists of two flat conductors separated by a thin strip of dielectric material. Tabs are formed on the conductors at various intervals as required (Figure 105).

Slip-on devices are connected to the tabs, thus making the assembly a pluggable device for use on the probe side of boards. Any number of slip-ons, up to eleven, may be installed on one assembly.

Application

The MINI-BUS may be used to distribute one special voltage and ground, or two special voltages.

Two to eleven slip-ons are located on the MINI-BUS assembly to satisfy the requirements of the application.

The MINI-BUS assembly is installed horizontally on the probe side of the board, between any two rows of pins. Connection to the laminar bus is by discrete wire.

Presently available are the following MINI-BUS configurations:

Part Number	Number of Positions
813263	2
813264	3
813265	4
813266	5
813267	6
813268	7
813269	8
813270	9
813271	10
811065	11

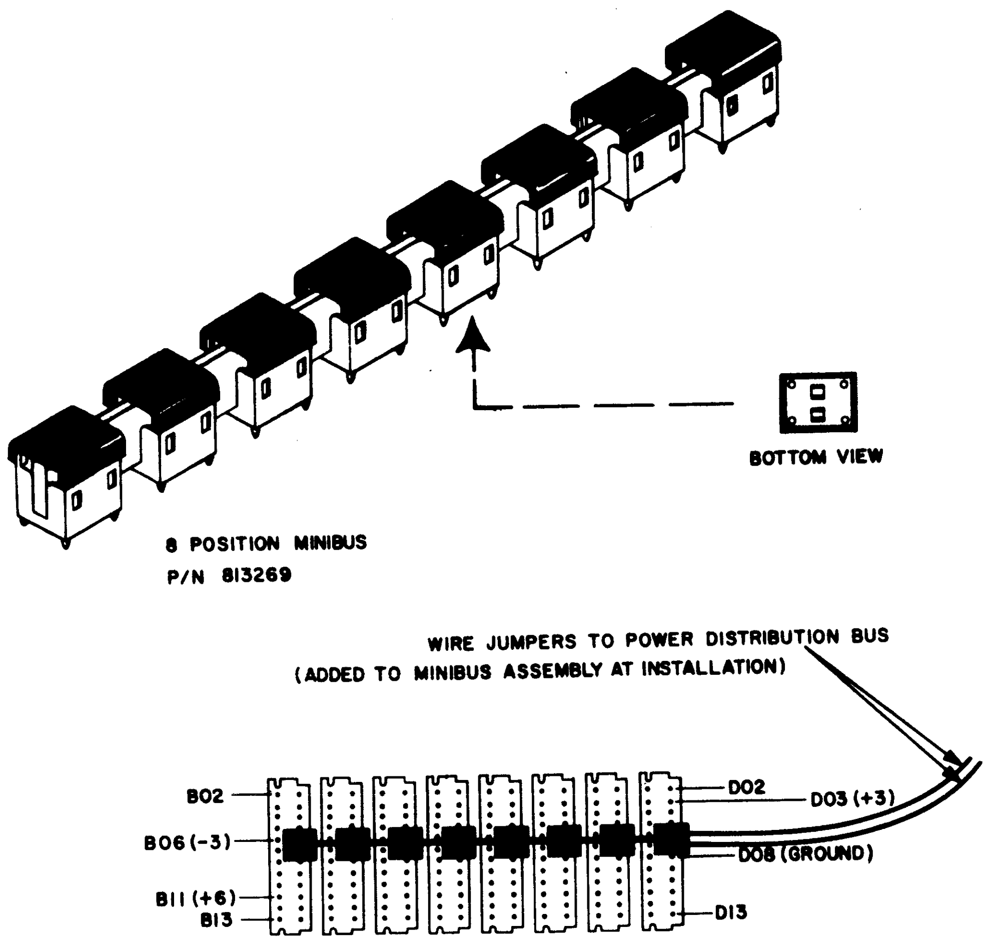


Figure 105. MINI-BUS

CHARACTERISTICS OF THE CONDUCTING MEDIA

	Specification Number	L (nh/inch)	C (pf/inch)	R_{dc} (milliohms/inch)	I (amps at 30°C)	C_{ww} (pf/inch)	C_{w-g} (pf/inch)	Short Circuit Current
Vertical Laminar Bus	890916	.606	117.8	.06	30			
Horizontal Laminar Bus	890916	.736	117.8	.05	40 50			
Voltage Crossover Bus to Board	890921	24.9 to 101		Pt. to Pt. 7	10			20 amp/sec
Voltage Crossover Board to Board	890921	36 to 130		Pt. to Pt. 12	10			20 amp/sec
MINI-BUS	890919	6.02	33.9	0.45	10			20 amp/sec
Internal +3 Volt Bus*	890909	1	40.0	Pt. to Pt. Res. 12	5			60 amp/200 millisec.
Internal +6 Volt Bus*	890909	1	40.0	Pt. to Pt. Res. 13	5			60 amp/200 millisec.
Internal -3 Volt Bus*	890909	3	13.0	Pt. to Pt. Res. 36	3			40 amp/200 millisec.
Internal Ground Plane**	890909			Pt. to Pt. Res. 6.2	*See Note			
0.010 Printed Line***	890914	11.25 to 12.9		29 to 36	1.0	.426 to .703	1.96 to 2.23	3.5 amps
0.030 Printed Line		6.97 to 7.63		7.5 to 7.8	3.0	.737 to 1.04	3.3 to 3.61	6.0 amps
Stranded Wire No. 18 AWG					8.0			
Stranded Wire No. 20 AWG					6.0			
Flat Cable	890917	10 to 11.7		18.75	1.0	.05 to .01	1 to 1.4	
Engineering Change Wire	890922							

Average Propagation Delay

Element	Delay
Board Printed Wiring	1.96 to 2.26 nsec/ft.
Card Printed Wiring (w/Internal Gnd.)	1.96 to 2.28 nsec/ft.
Card Printed Wiring	0.106 nsec/inch
Spring (Card Contact)	0.120 nsec/spring
Board Discrete Wiring	1.300 to 1.500 nsec/ft.
Flat Cable	1.400 to 1.600 nsec/ft.

Contact Resistance

1. Crossover Connector (Voltage) - 5 milliohms/contact
2. Card Socket - 10 milliohms/contact

---

*Each leg of internal bus.
**Must carry return currents of -3, +3, and +6 volt supplies.
***Based on 0.010" spacing.

REFERENCE SECTION

(Card Flyers and Schematics - Numerically by Part Number)

Contains logic diagrams and schematics for those logic cards considered to be basic building blocks. Where both the schematic and logic diagram are available, the schematic follows the logic diagram.

LOGIC GENERAL FORM - XYYZZ

X DEFINED

S - SRETL GENERAL
T - 30 NS
U - 5-10 NS
V - 700 NS
O - ANALOG

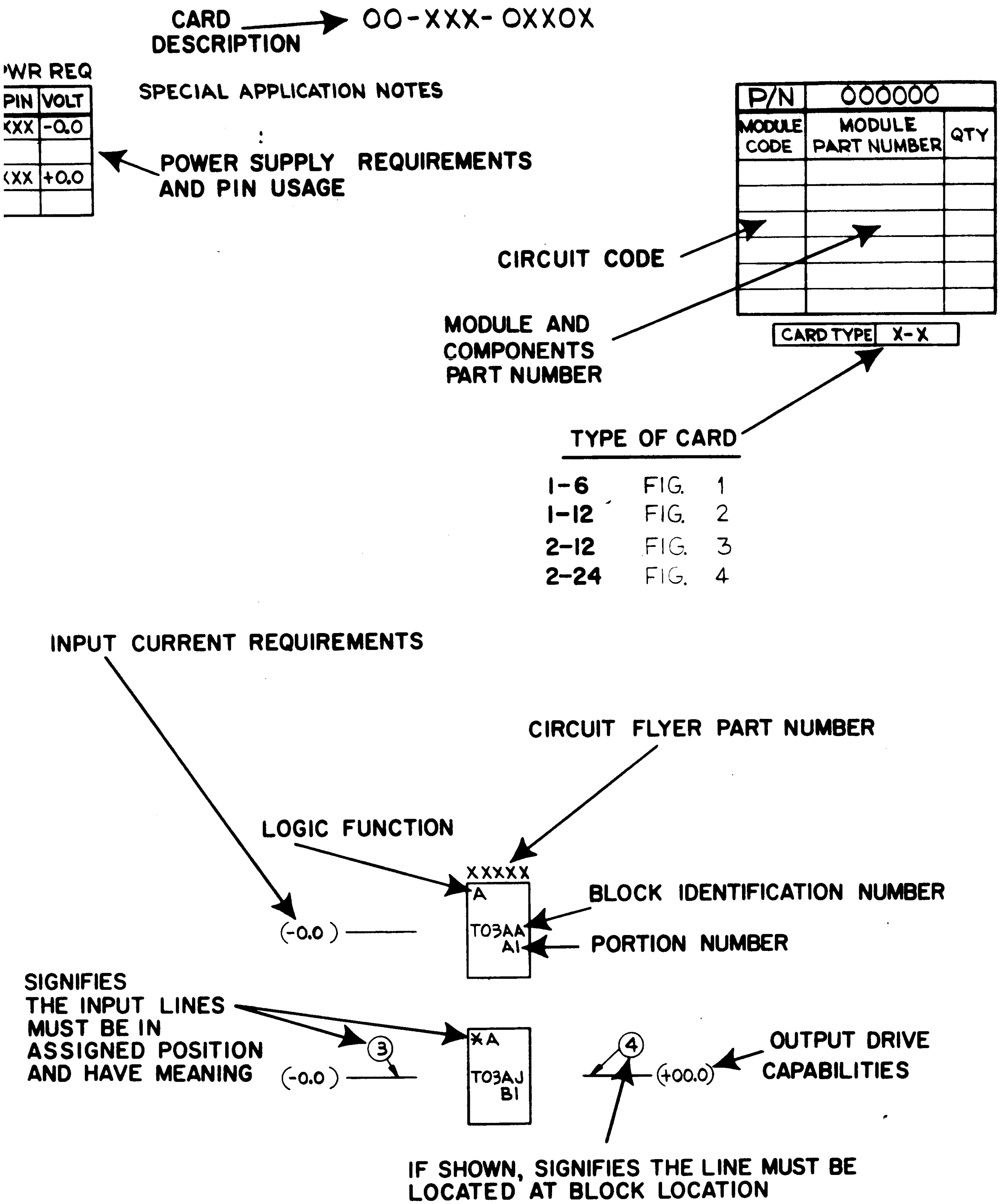
YY DEFINED

3 - LOGIC BLOCKS
5 - VOLTAGE TRANSLATE CIRCUITS
6 - TRANSMISSION LINE DRIVERS AND RECEIVERS
7 - SENSE AMPLIFIERS
10 - INVERTING DRIVERS LESS THAN 50 MA
11 - NON-INVERT DRIVER LESS THAN 50 MA
15 - POWER DRIVER MORE THAN 50 MA
16 - MAGNETIC HEAD AND CORE DRIVER
20 - TRIGGERS
21 - SINGLESHOTS
22 - OSCILLATORS
25 - REGULATORS, CLAMPS, CLIPPERS, AND LIMITERS
32 - GATES
40 - SPECIALS
45 - DELAY CIRCUITS
55 - INDICATOR CIRCUITS
60 - INTEGRATORS AND FILTERS
61 - COMPONENTS
63 - REED RELAYS
65 - FUNCTIONAL CARD
66 - FIELD REPLACEMENT CARD

ZZ DEFINED - THE UNIQUE CIRCUIT

CIRCUIT NUMBER	TITLE	CIRCUIT NUMBER	TITLE
T03AJ	AND-PWR INVERT 300 OHM LOAD	T05AL	TRANSLATE BLOCK
T03AK	EXCLUSIVE OR LATCH	T05AM	WRITE DRIVER CHECK
T03AL	8 WAY EXCLUSIVE OR	T05AO	45 MA TRANSMISSION LINE DRIVER
T03AM	4 WAY EXCLUSIVE OR	T05AP	INTERLOCK CIRCUIT TERMINATOR
T03AN	7 WAY API-NO LOAD	T05AQ	INVERTER

●FIGURE 106. An Example of the Circuit Number Listing



ALL LOGIC PAGES AND SCHEMATICS IN THIS MANUAL WILL BE IN PART NUMBER ORDER. EACH LOGIC PAGE SHOULD BE FOLLOWED BY ITS SCHEMATIC.

FIGURE 107: KEY TO INTERPRETING CARD LOGIC DIAGRAMS

2-3AI W/L AND 4-2AI-W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES:

P/N	5800000	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	6

CARD TYPE 1-6

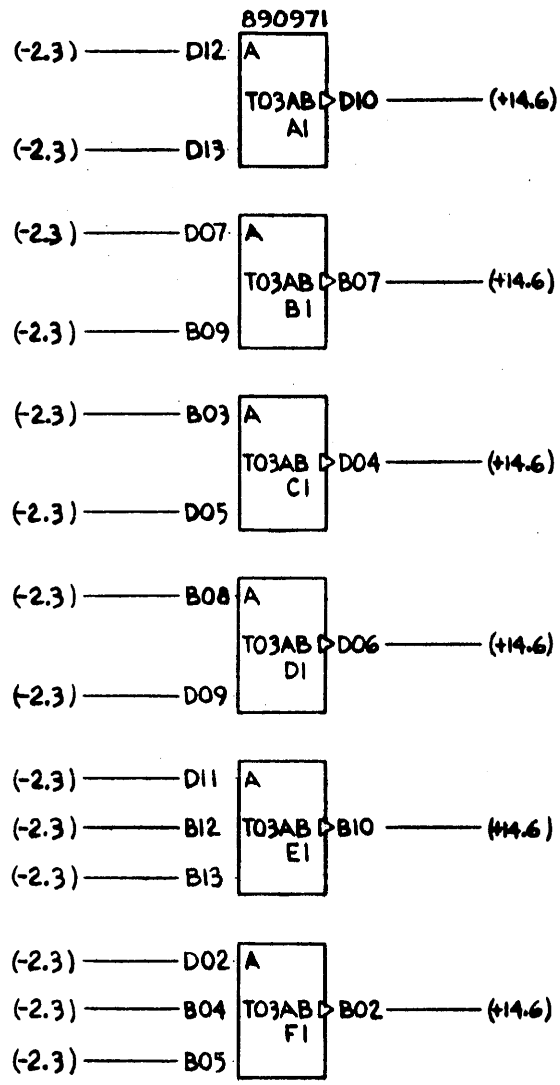


FIGURE 108

2-3AI W/L AND 4-2AI-W/L

P/N 5800000

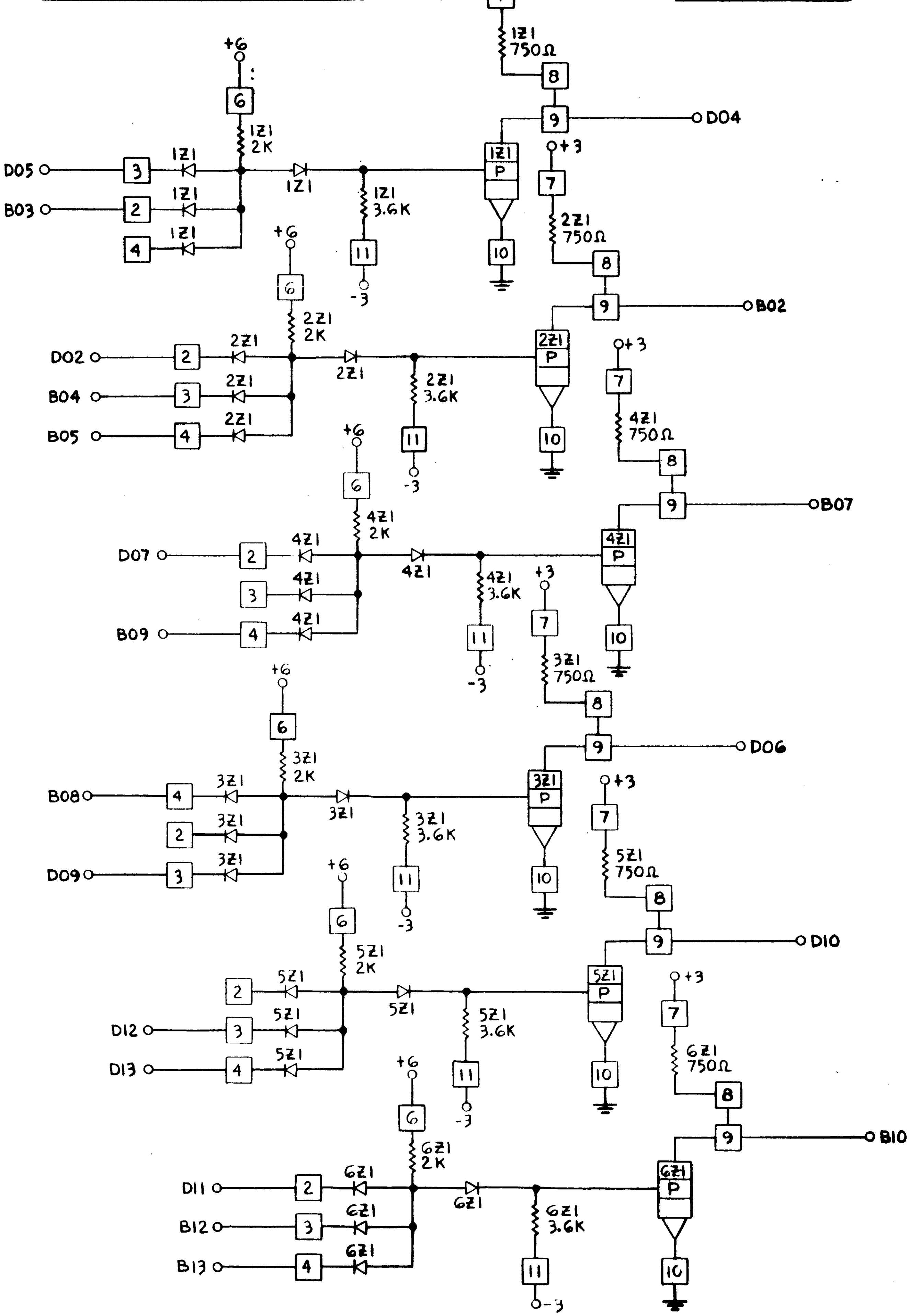


FIGURE 109

PWR REQ

PIN	VOLT
D08	GRD
D03	+ 3
B11	+ 6
B06	- 3

SPECIAL APPLICATION NOTES

P/N	5800002	
MODULE CODE	MODULE PART NUMBER	QTY
A1	361451	5

CARD TYPE	1-6

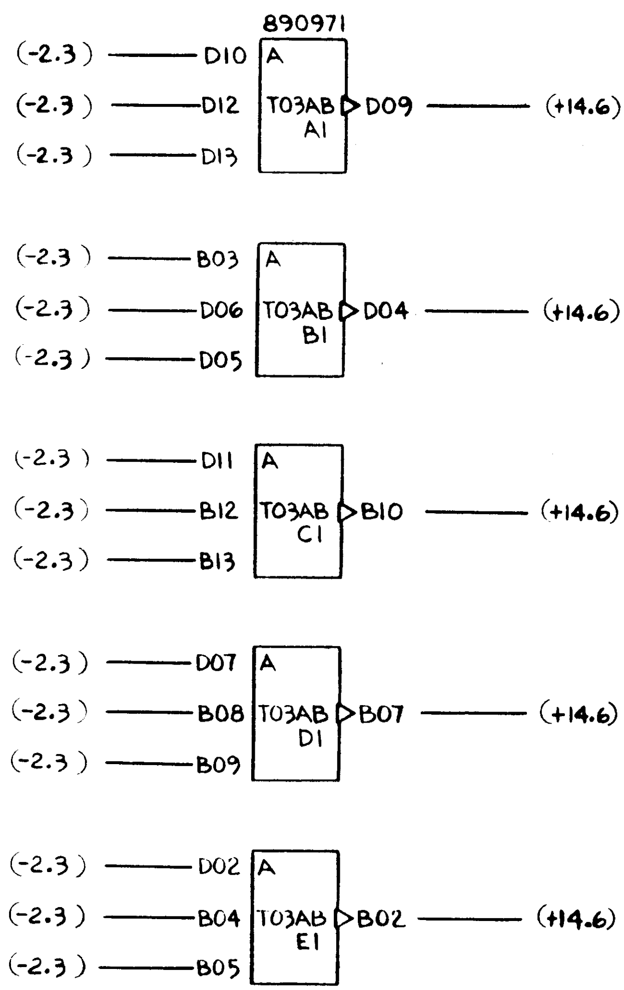


FIGURE 110

5-3WAI W/L P/N 5800002

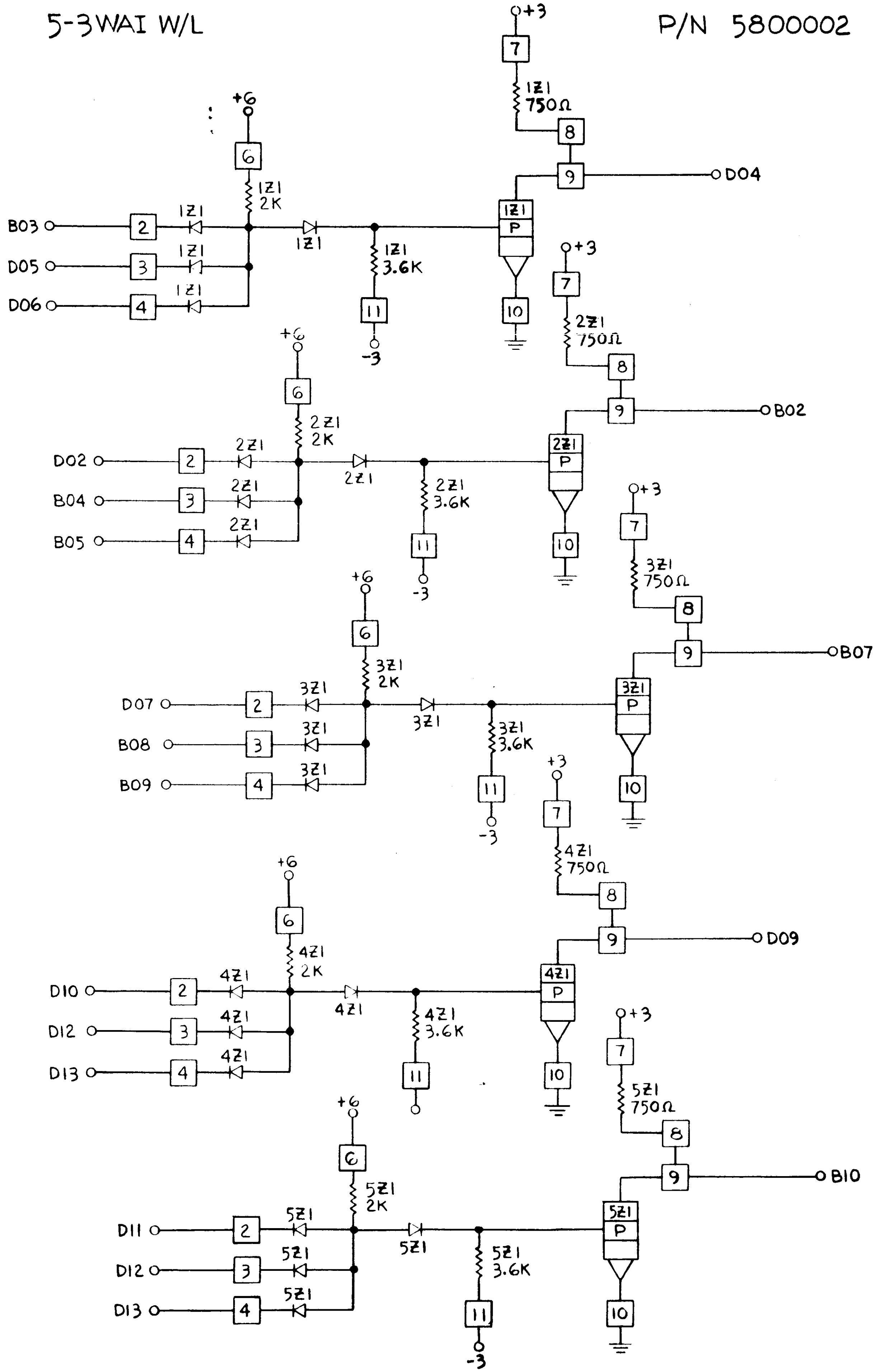


FIGURE 111

2-7WAI W/L + 3WAI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800004	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	3
FDD	361459	1

CARD TYPE	1-6

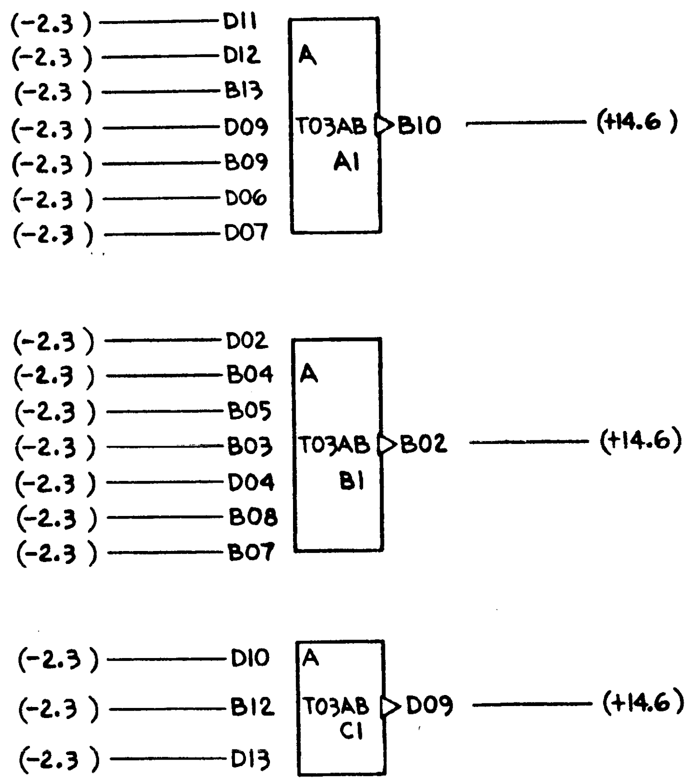


FIGURE 112

2-7WAI W/L+3WAI W/L

P/N 5800004

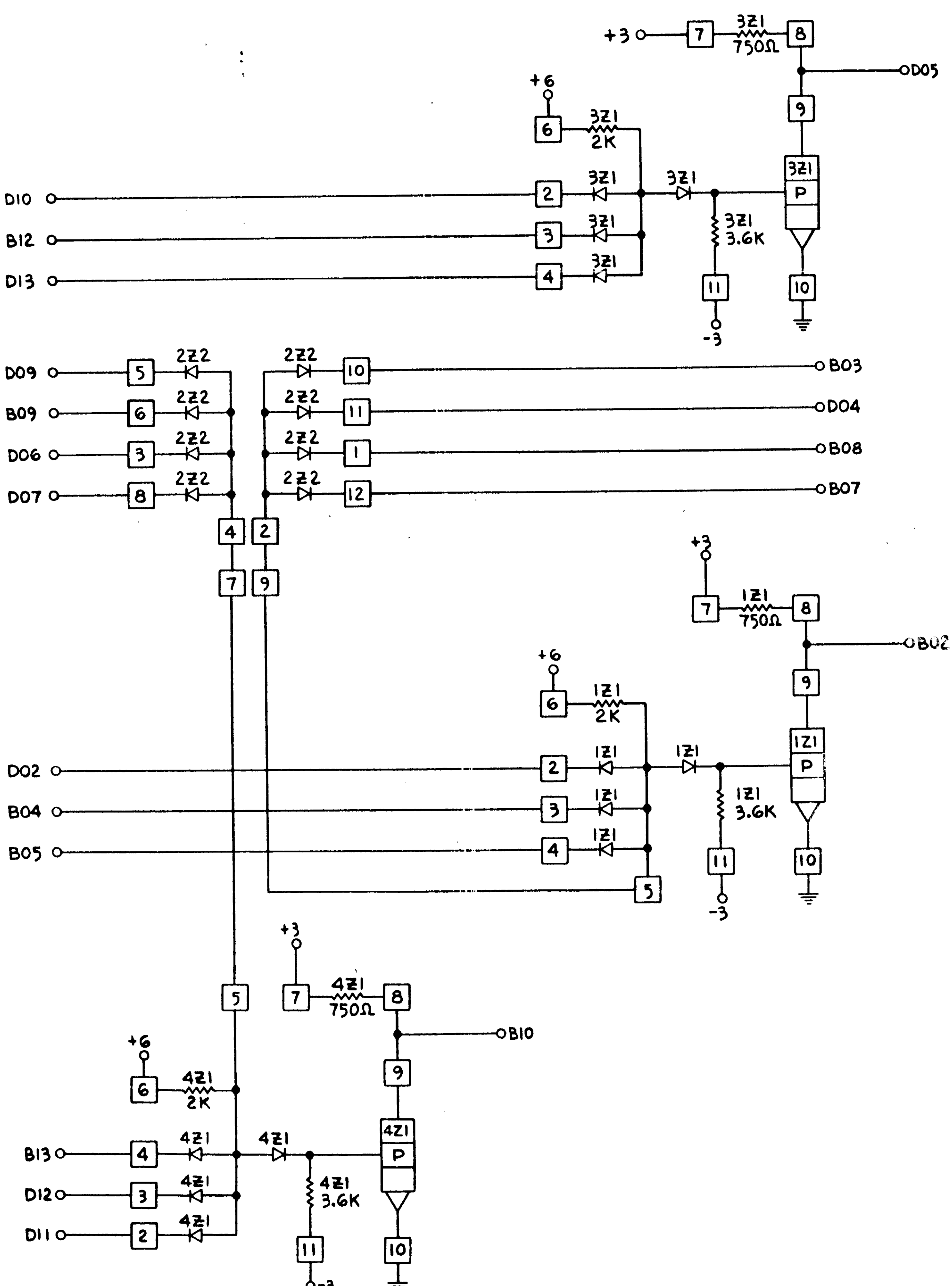


FIGURE 113

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1-11WAI W/L+ 2-3WAI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B6	-3

SPECIAL APPLICATION NOTES

P/N	5800005	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	3
FDD	361459	1

CARD TYPE	1H6

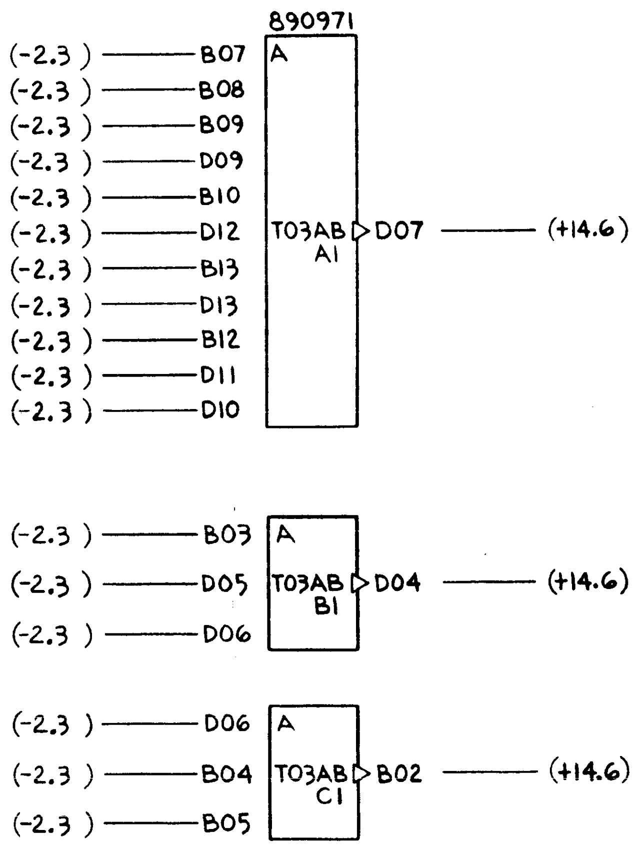


FIGURE 114

1-11WAI W/L+ 2-3WAI W/L P/N 5800005

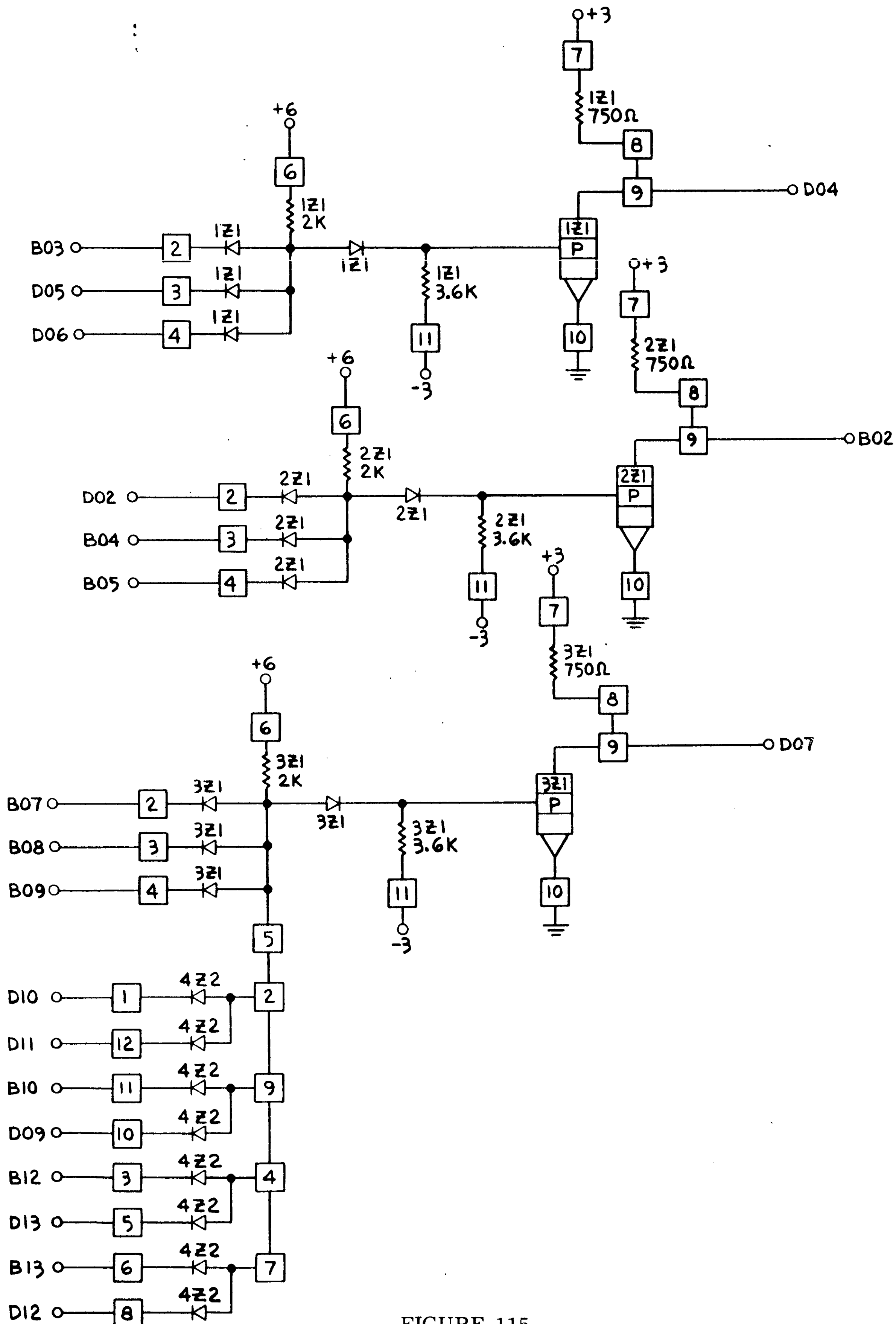


FIGURE 115

4-2 INPUT-2 WAY AND OR INVERT W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800006	
MODULE CODE	MODULE PART NUMBER	QTY
AOI	361453	4
AOXB	361456	2

CARD TYPE	1-6

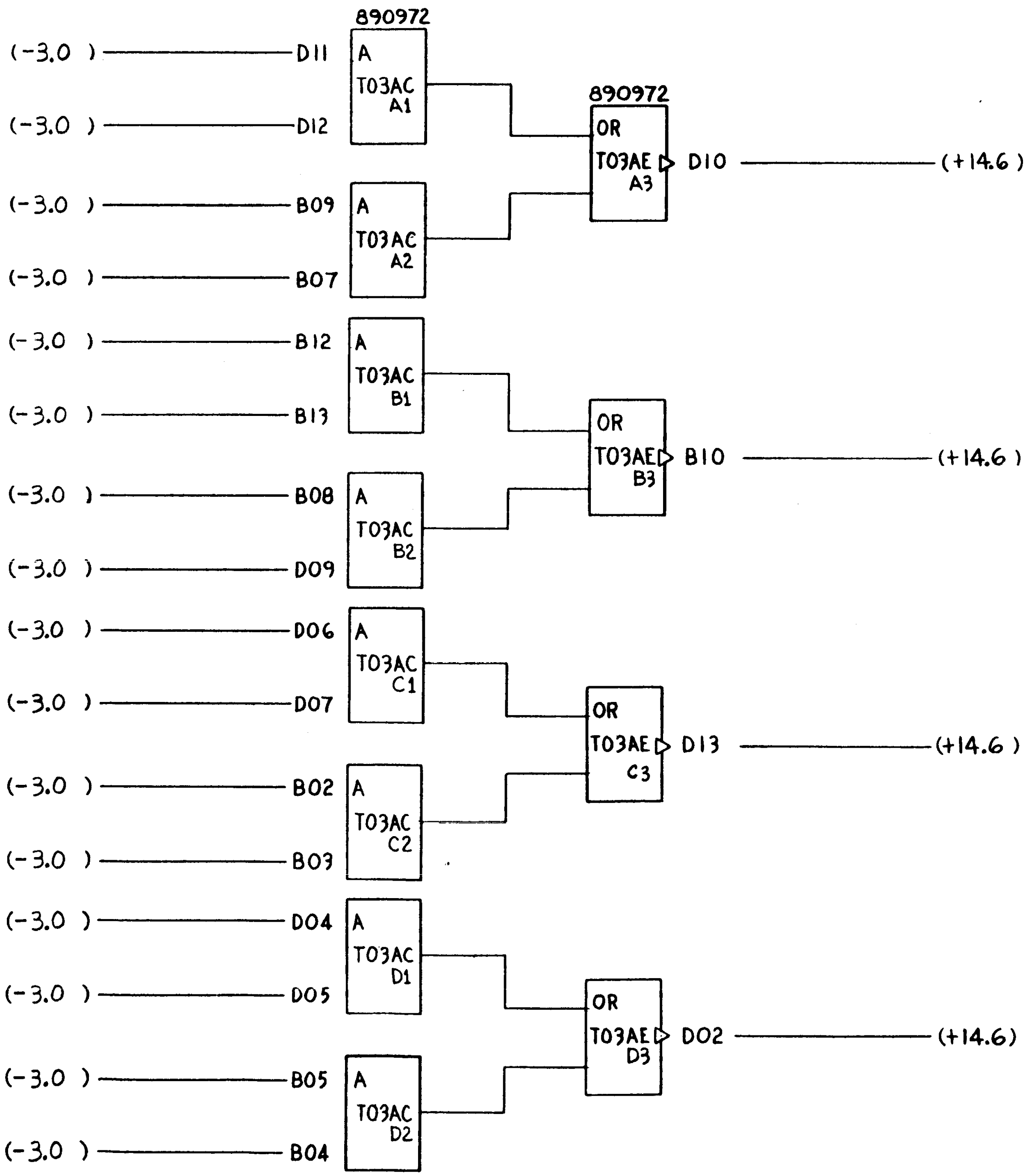


FIGURE 116

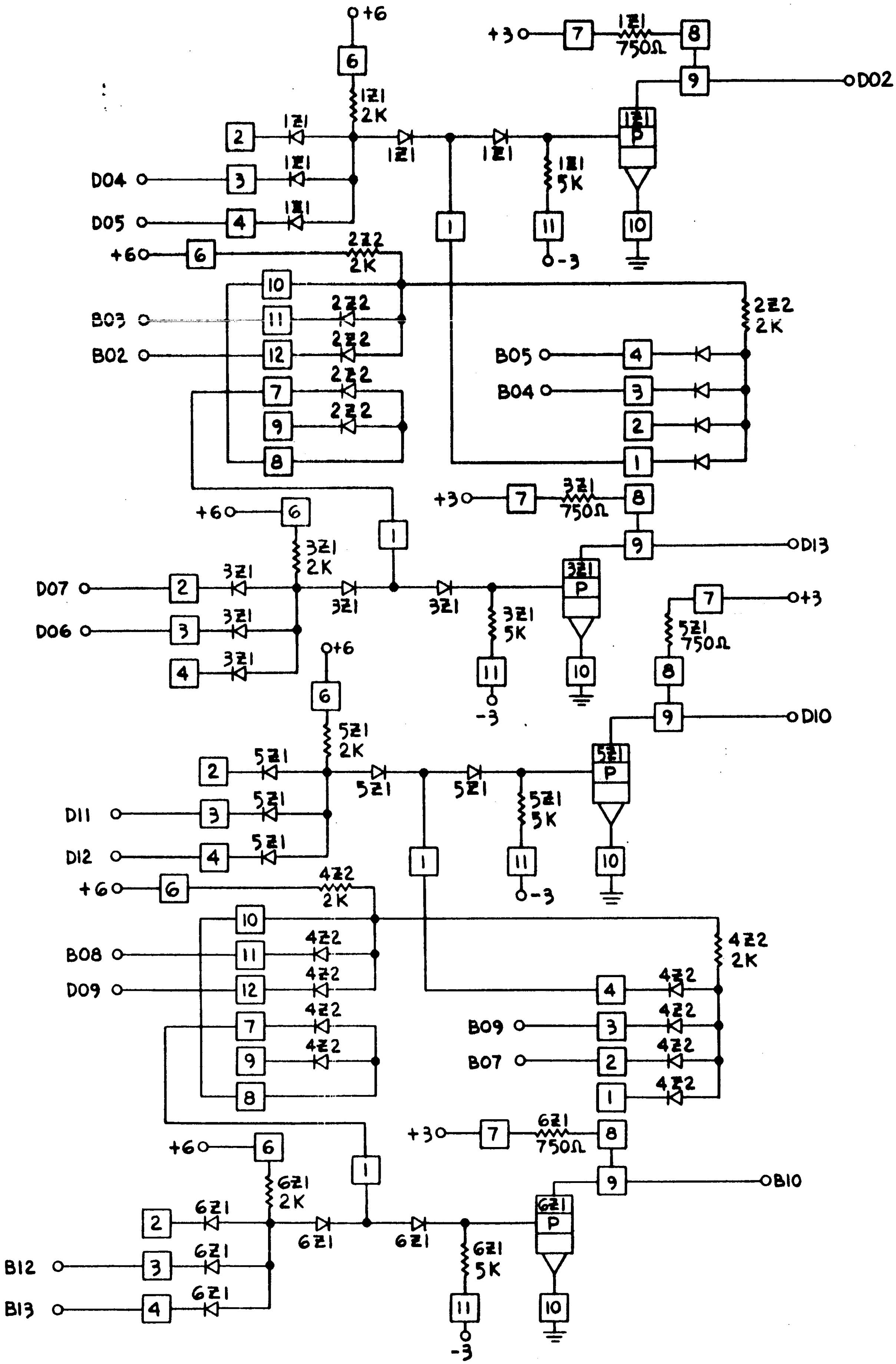

+6
+3
1Z1
750Ω
D02
2K
D04
D05
5K
-3
2Z2
B03
B02
B05
B04
3Z1
D13
D07
D06
5Z1
D10
D11
D12
4Z2
B08
D09
B09
B07
6Z1
B10
B12
B13
P

FIGURE 117

2-(2-3WAOI W/L+ 2-2WAI W/L)

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800007	
MODULE CODE	MODULE PART NUMBER	QTY
AOI	361453	2
AOXB	361456	1
AI	361451	2

CARD TYPE	1-6

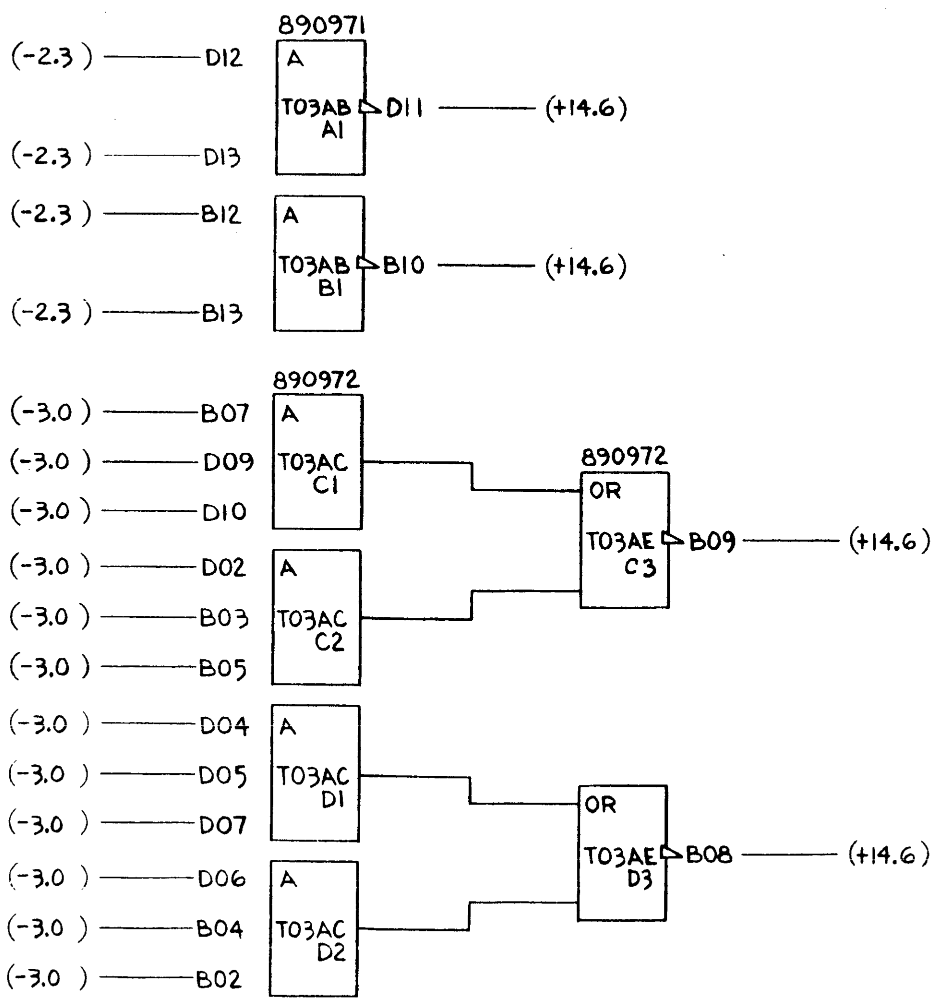


FIGURE 118

2-(2-3WAOI W/L + 2-2 WAI W/L) P/N 5800007

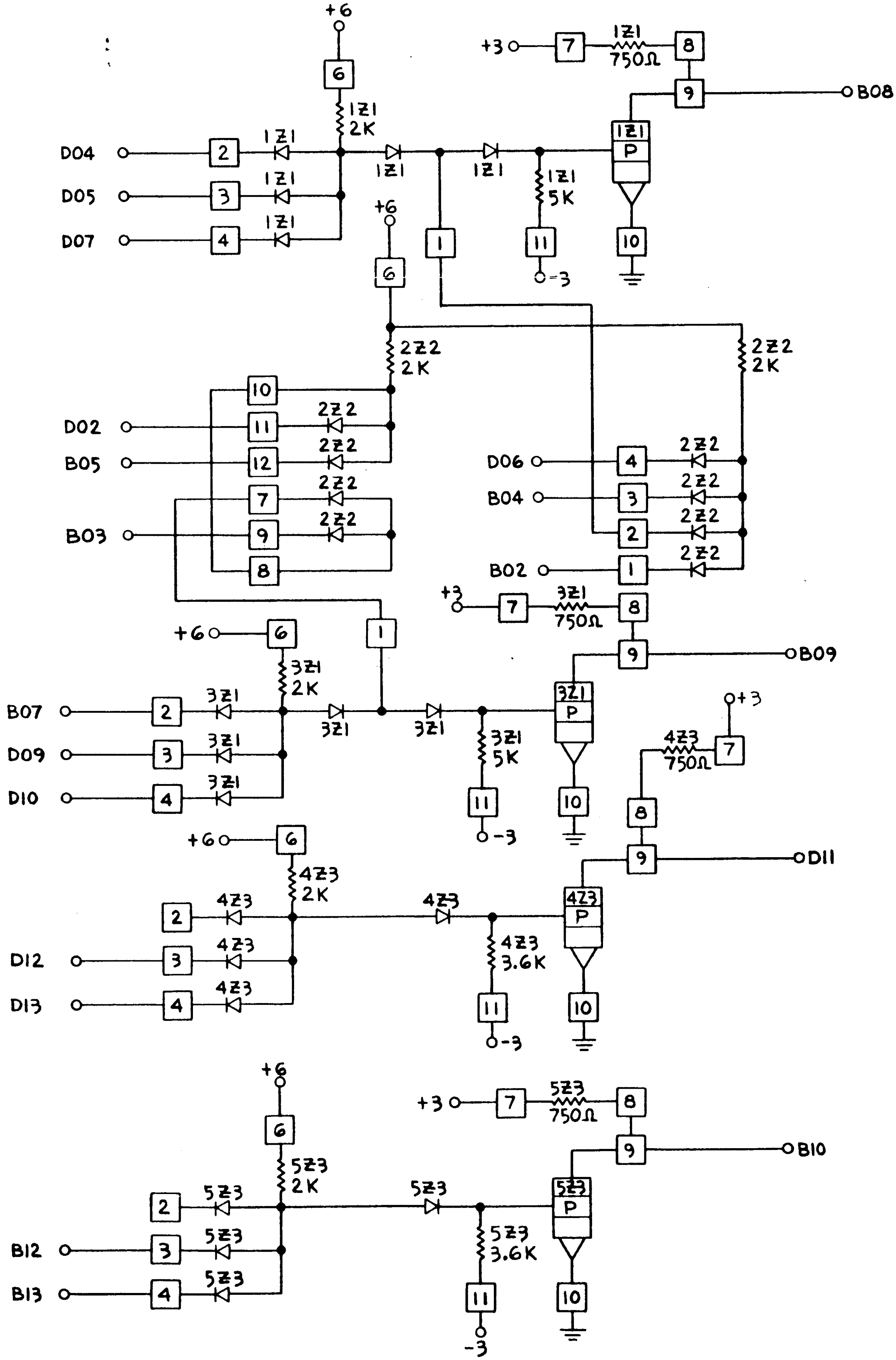


FIGURE 119

2 (3-3 WAOI W/L)

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800008	
MODULE CODE	MODULE PART NUMBER	QTY
AOI	361453	2
AOXB	361456	2

CARD TYPE	1-6

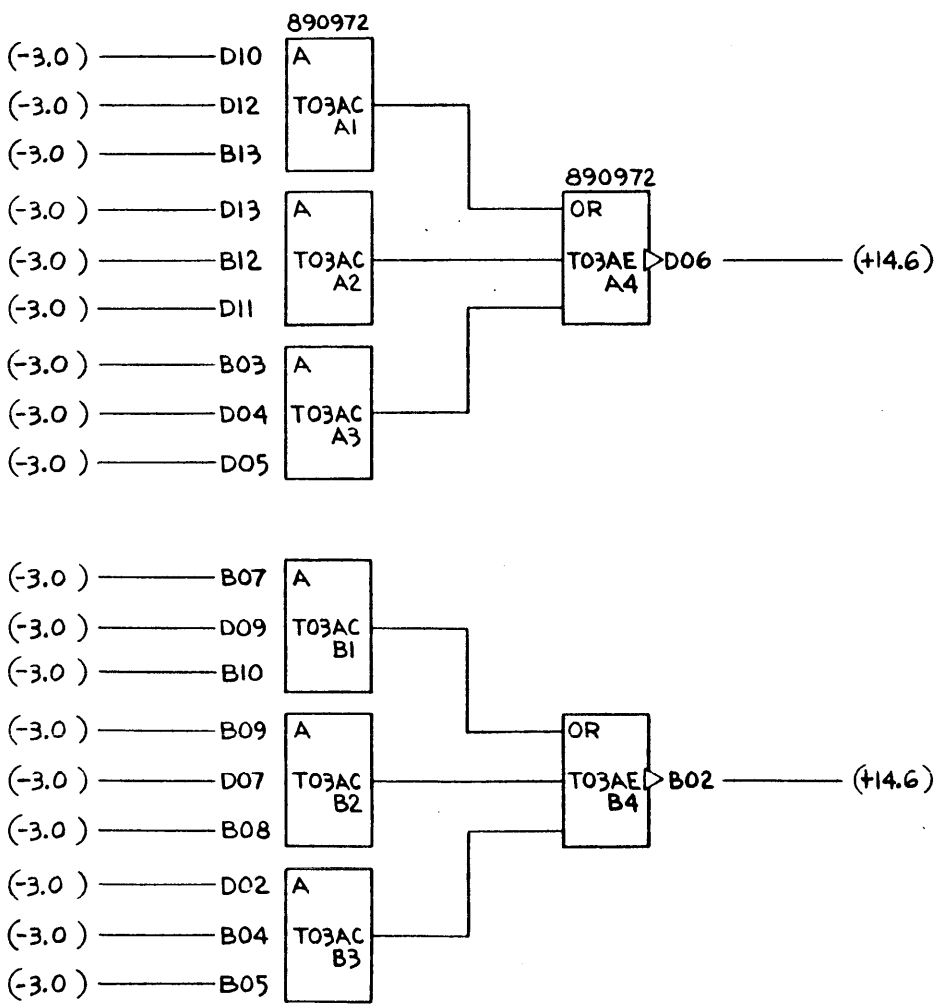


FIGURE 120

2 (3-3WAOI W/L) P/N 5800008

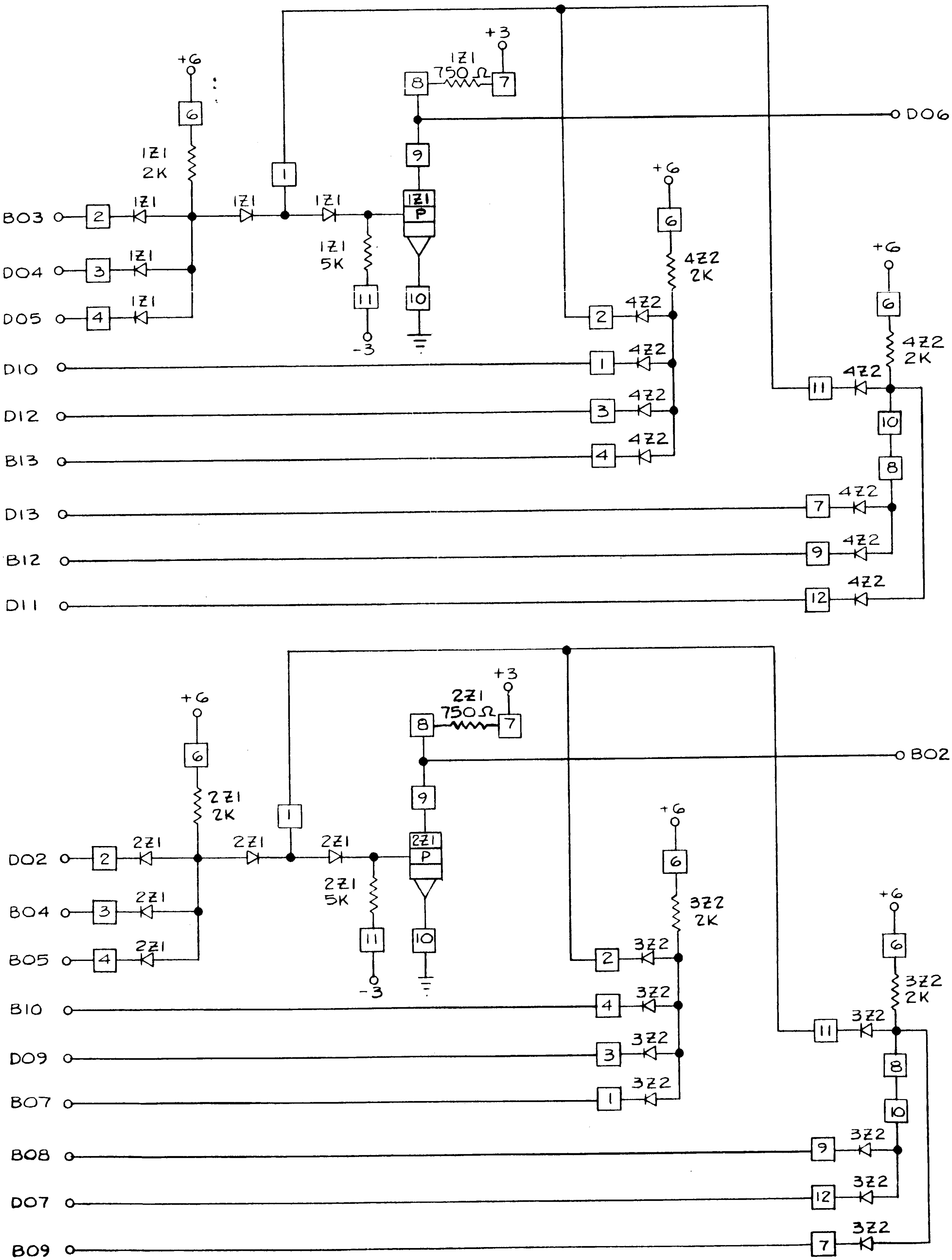


FIGURE 121

10-DIRECT COUPLED INVERTERS

PWR REQ

PIN	VOLT
D08	GRD
D03	+3

SPECIAL APPLICATION NOTES

:

P/N	5800009	
MODULE CODE	MODULE PART NUMBER	QTY
DCI	361454	5

CARD TYPE	1-6

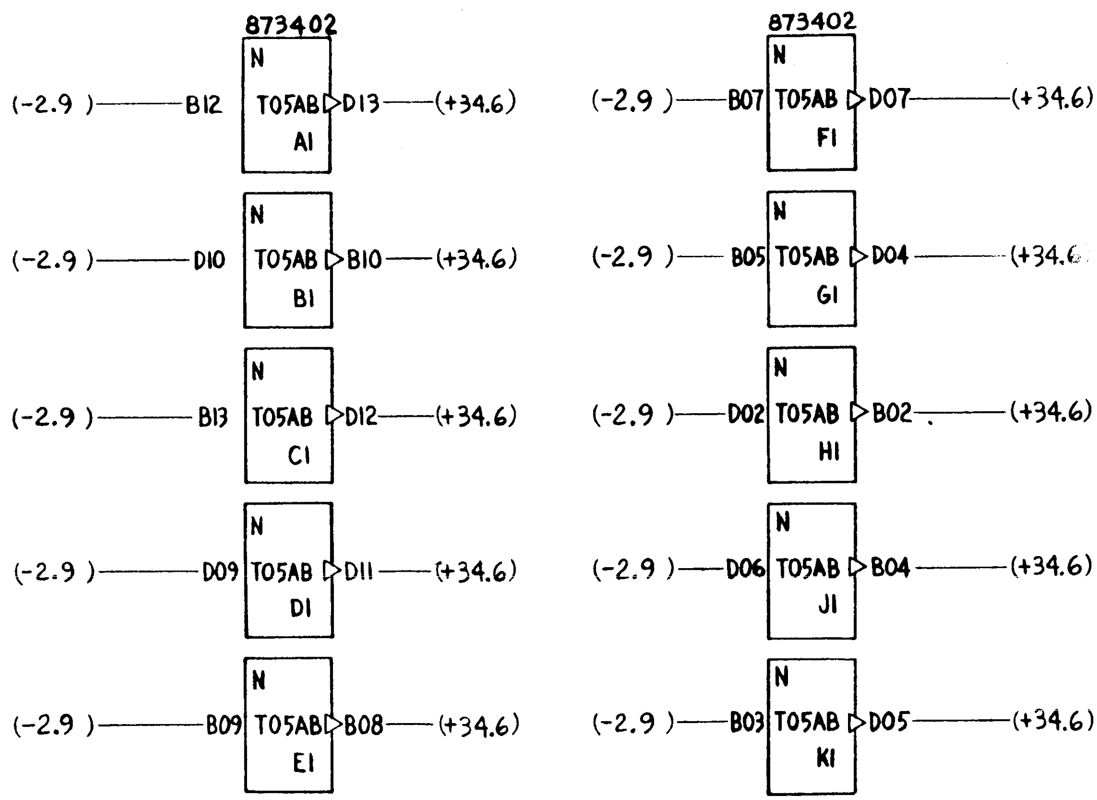


FIGURE 122

10-DIRECT COUPLED INVERTERS P/N 5800009

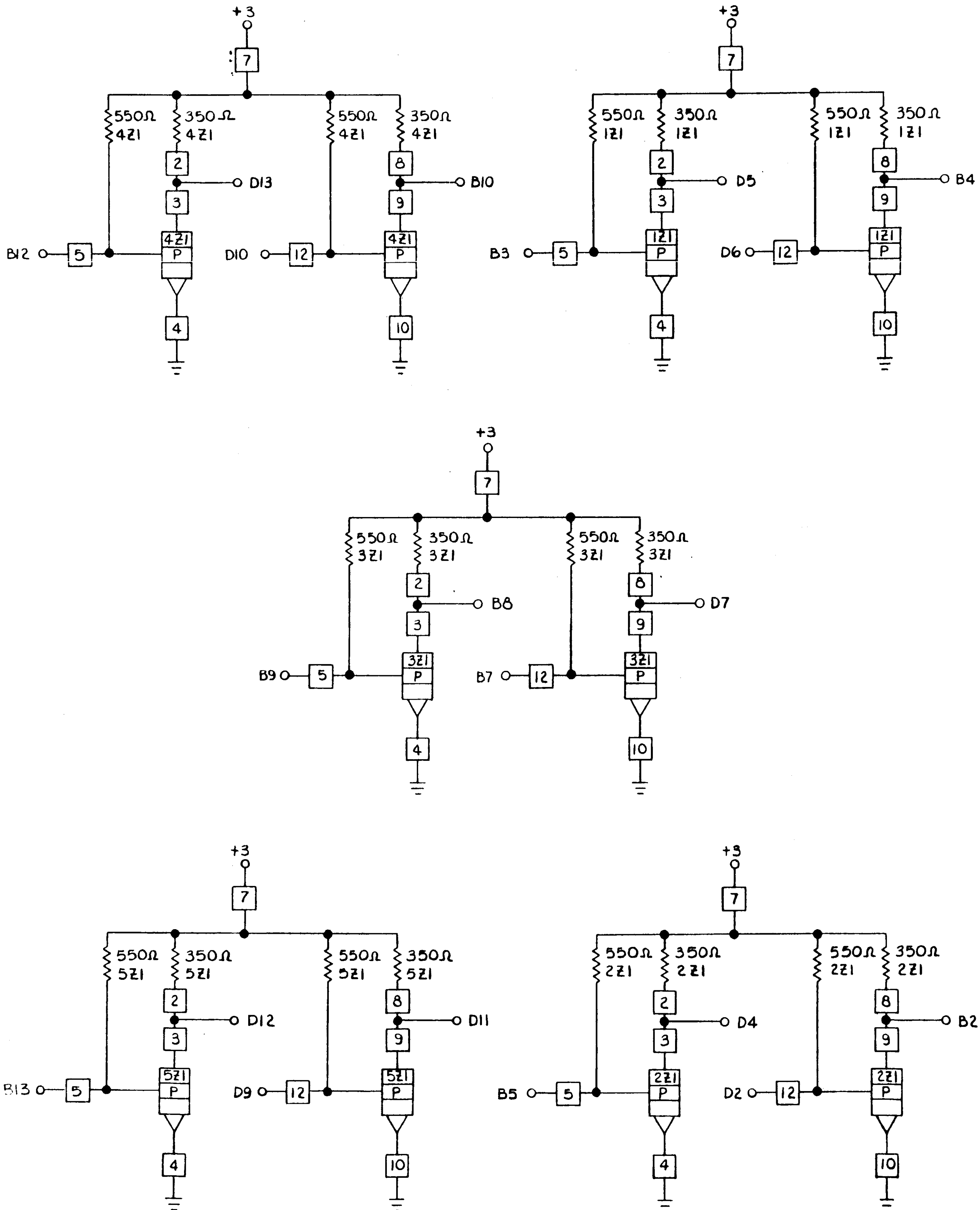


FIGURE 123

1-[5-3WAOI W/L]+ 21WAI W/L

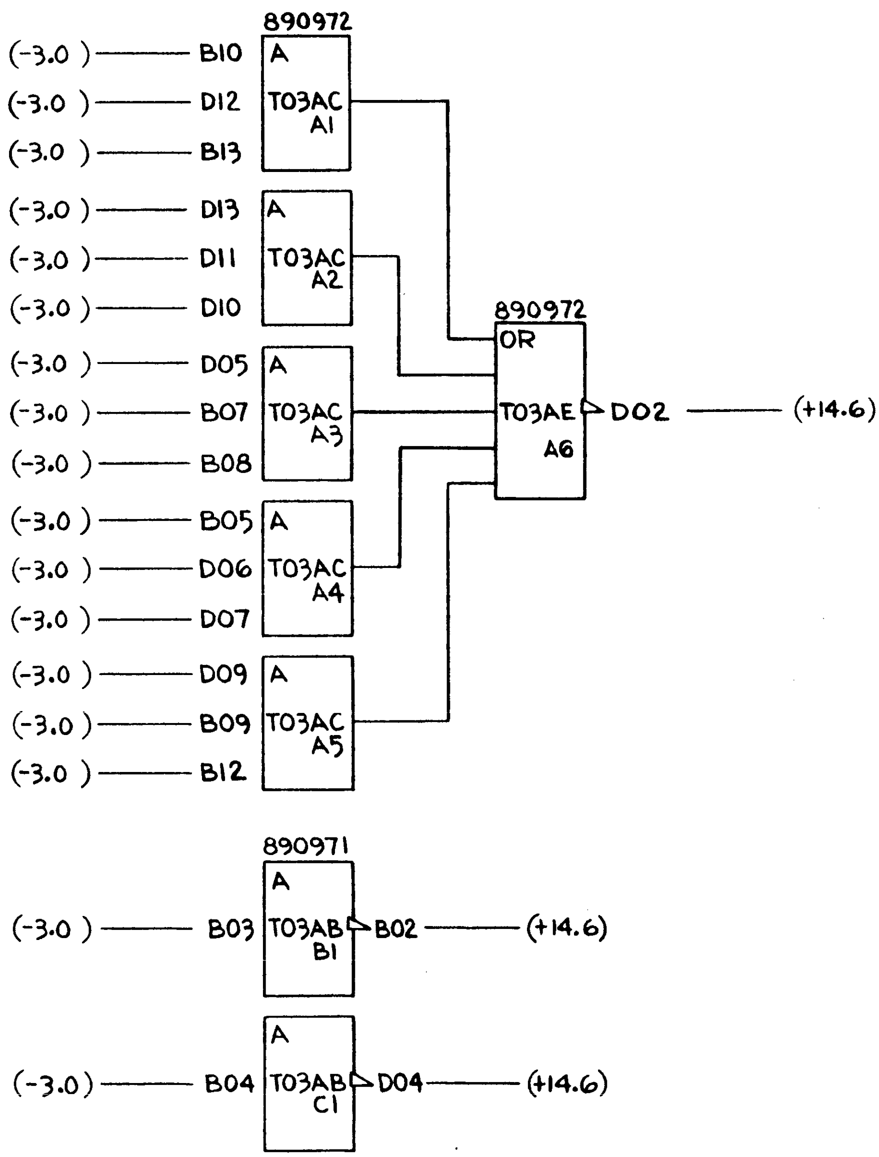
PWR REQ

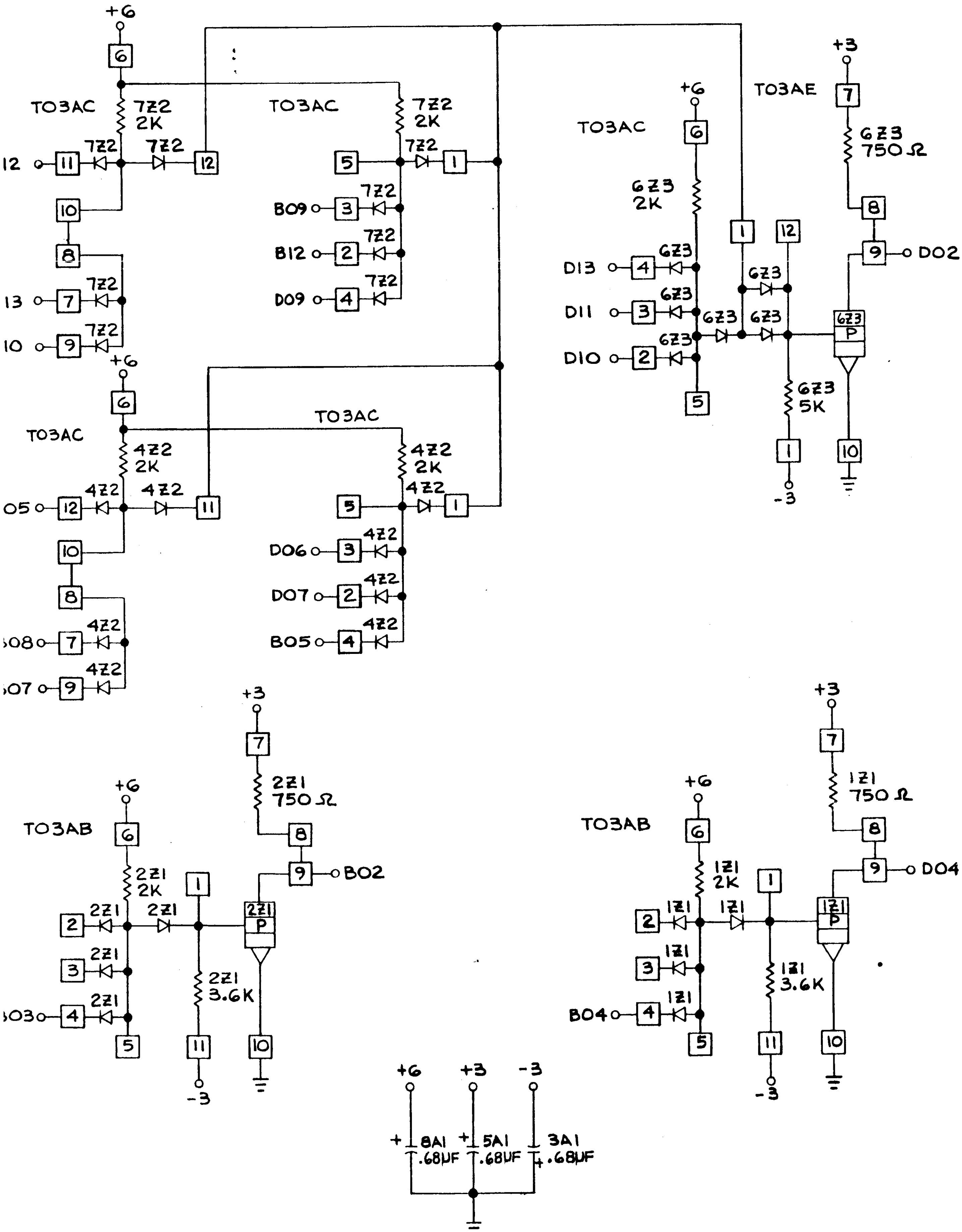
PIN	VOLT
D08	GRD
D03	+ 3
B11	+ 6
B06	- 3

SPECIAL APPLICATION NOTES

P/N	5800066	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	2
AOXB	361456	2
AOI	361453	1
	2414883	3

CARD TYPE	1-6




+6
TO3AC
7Z2
2K
TO3AE
+3
750 Ω
6Z3
5K
D13
D11
D10
D02
B09
B12
D09
4Z2
D05
D06
D07
B05
TO3AB
2Z1
3.6K
B02
B03
1Z1
D04
B04
-3
8A1
5A1
3A1
.68UF

PWR REQ

PIN	VOLT
D08	GND
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800069	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	4
FDD	361459	1

CARD TYPE	1-6

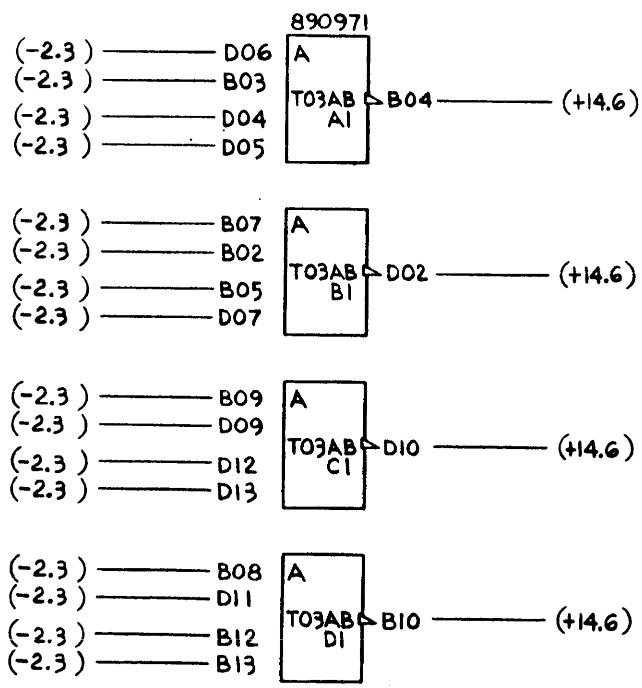


FIGURE 126

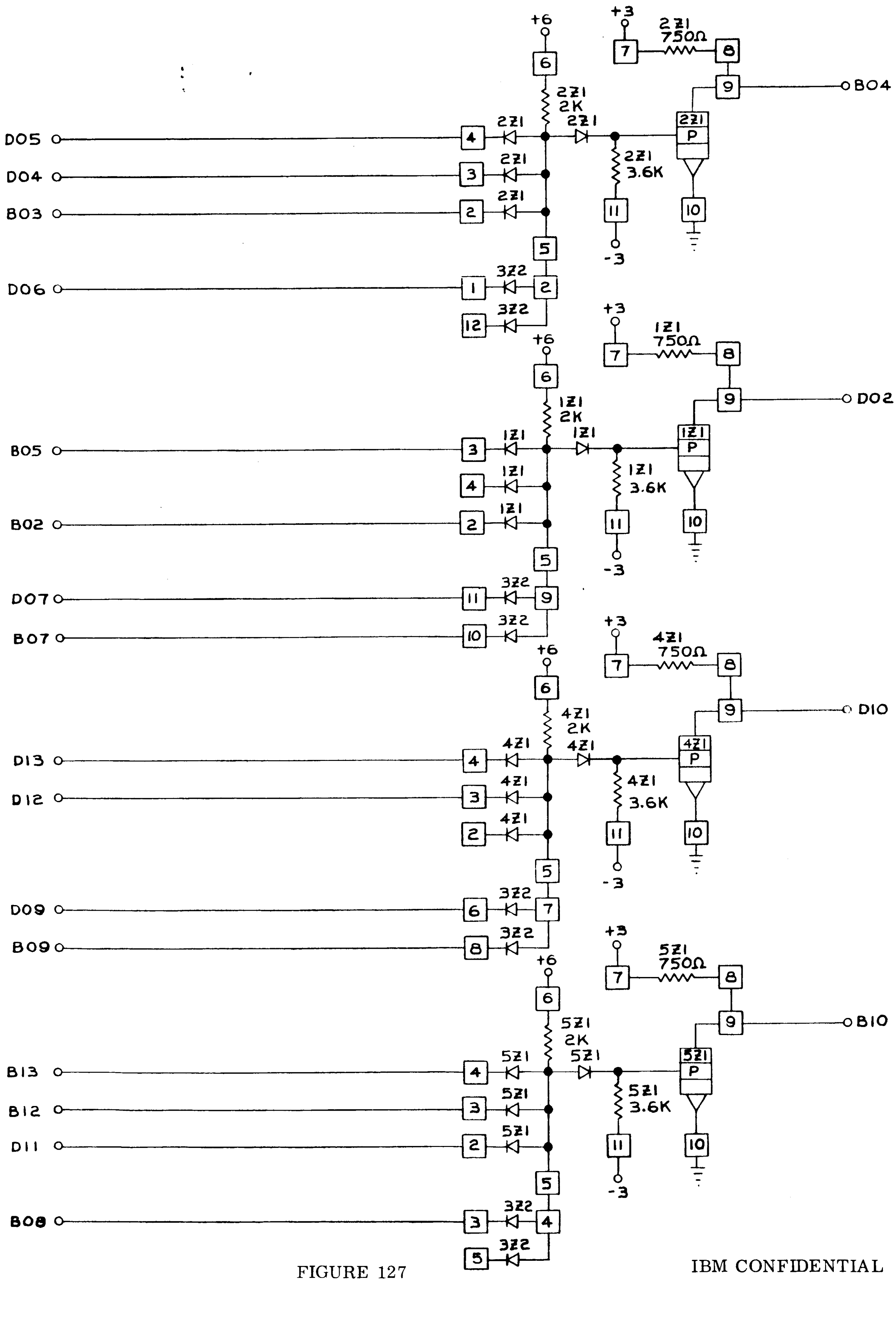

+6
+3
2Z1
750Ω
B04
2Z1
2K
D05
D04
B03
D06
3Z2
2Z1
3.6K
-3
+3
1Z1
750Ω
D02
1Z1
2K
B05
B02
1Z1
3.6K
D07
B07
3Z2
+3
4Z1
750Ω
D10
4Z1
2K
D13
D12
4Z1
3.6K
D09
B09
3Z2
+3
5Z1
750Ω
B10
5Z1
2K
B13
B12
D11
5Z1
3.6K
B08
3Z2
P

FIGURE 127

PWR REQ

PIN	VOLT
D08	GRD
D11	+6
D03	+3
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800097	
MODULE CODE	MODULE PART NUMBER	QTY
FDD	361459	2
AI	361451	1
	2414883	3

CARD TYPE	1-6

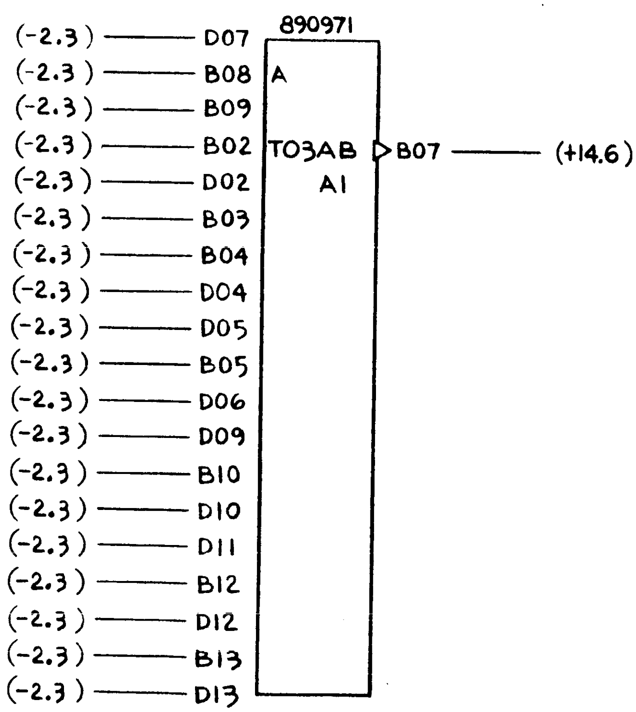


FIGURE 128

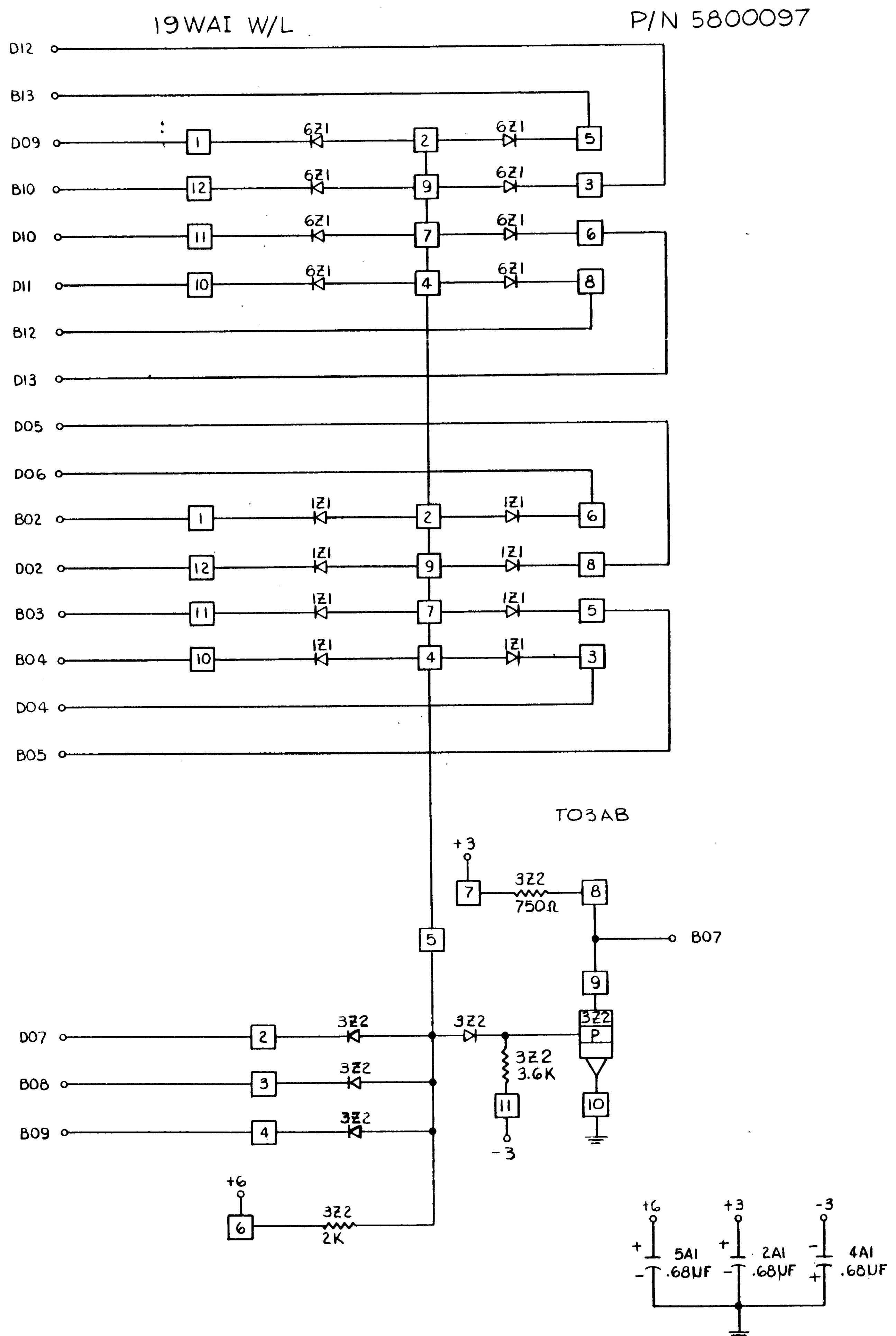

19WAI W/L
P/N 5800097
D12
B13
D09
B10
D10
D11
B12
D13
D05
D06
B02
D02
B03
B04
D04
B05
6Z1
1Z1
TO3AB
+3
3Z2
750Ω
B07
D07
B08
B09
3Z2
3.6K
-3
+6
2K
P
+6
+3
-3
5A1
.68UF
2A1
.68UF
4A1
.68UF

FIGURE 129

2-3WAPI W/L + 4-2WAPI W/L

PWR REQ

PIN	VOLT
D03	+3
D08	GRD
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800199	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	6
	2414883	1

CARD TYPE	1-6

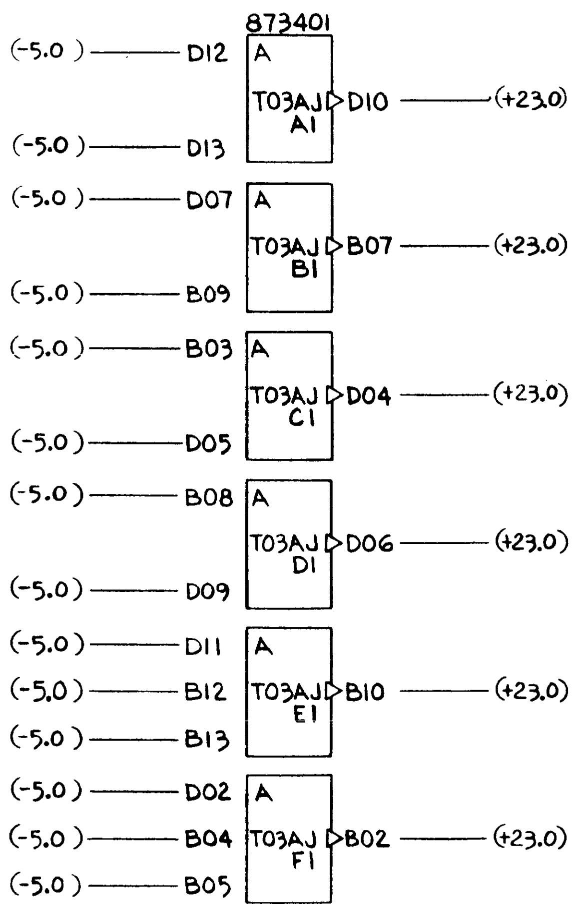


FIGURE 130

2-3 WAPI W/L + 4-2 WAPI W/L P/N 5800199

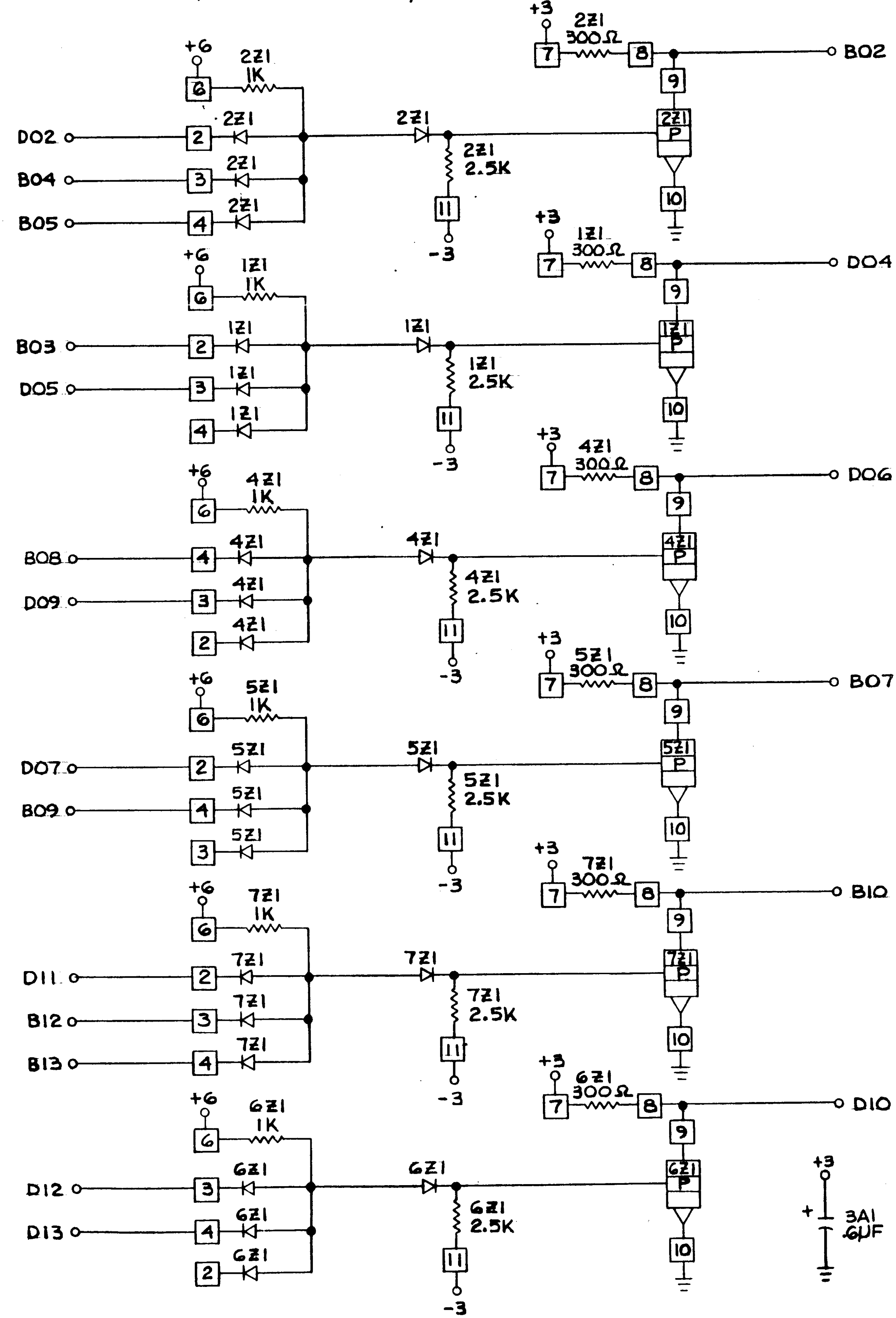


FIGURE 131

5-3WPI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+ 3
B11	+ 6
B06	- 3

SPECIAL APPLICATION NOTES

P/N	5800200	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	5
	2414883	1

CARD TYPE	1-6

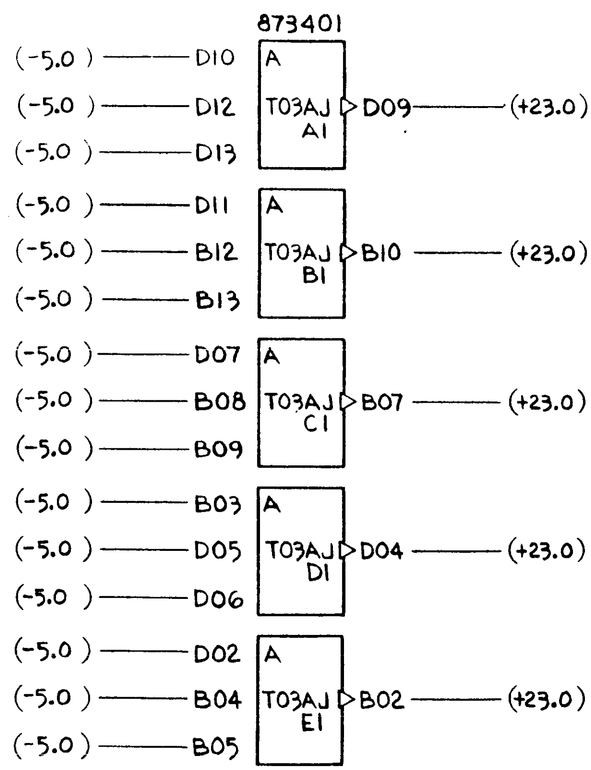


FIGURE 132

5-3WPI W/L

P/N 5800200

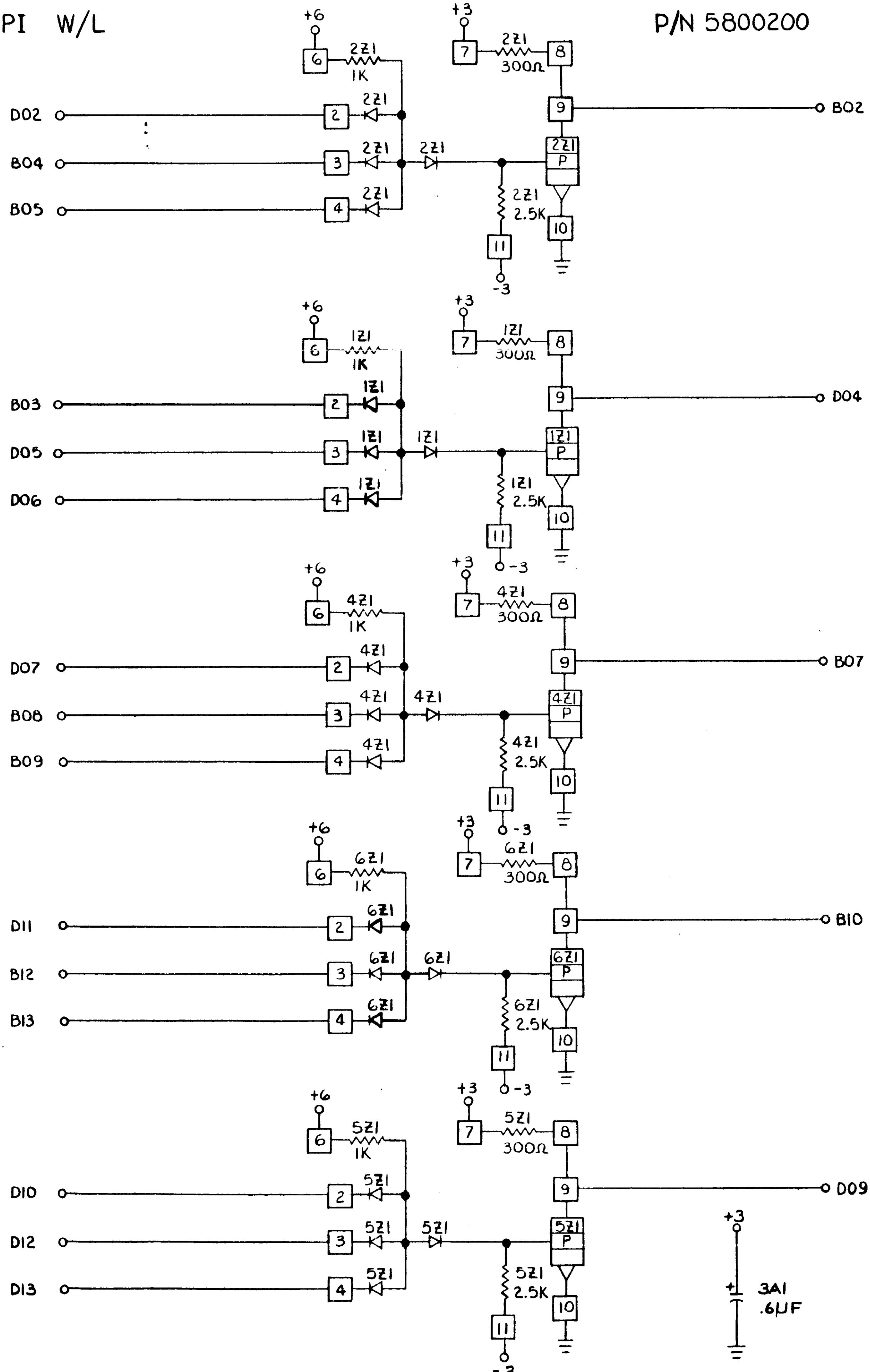


FIGURE 133

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2-[3-2WAOI W/L] 2-2WAI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+ 3
B11	+ 6
B06	- 3

SPECIAL APPLICATION NOTES

P/N	5800212	
MODULE CODE	MODULE PART NUMBER	QTY
AOX	361455	2
AI	361451	2
AOI	361453	2

CARD TYPE	1-6

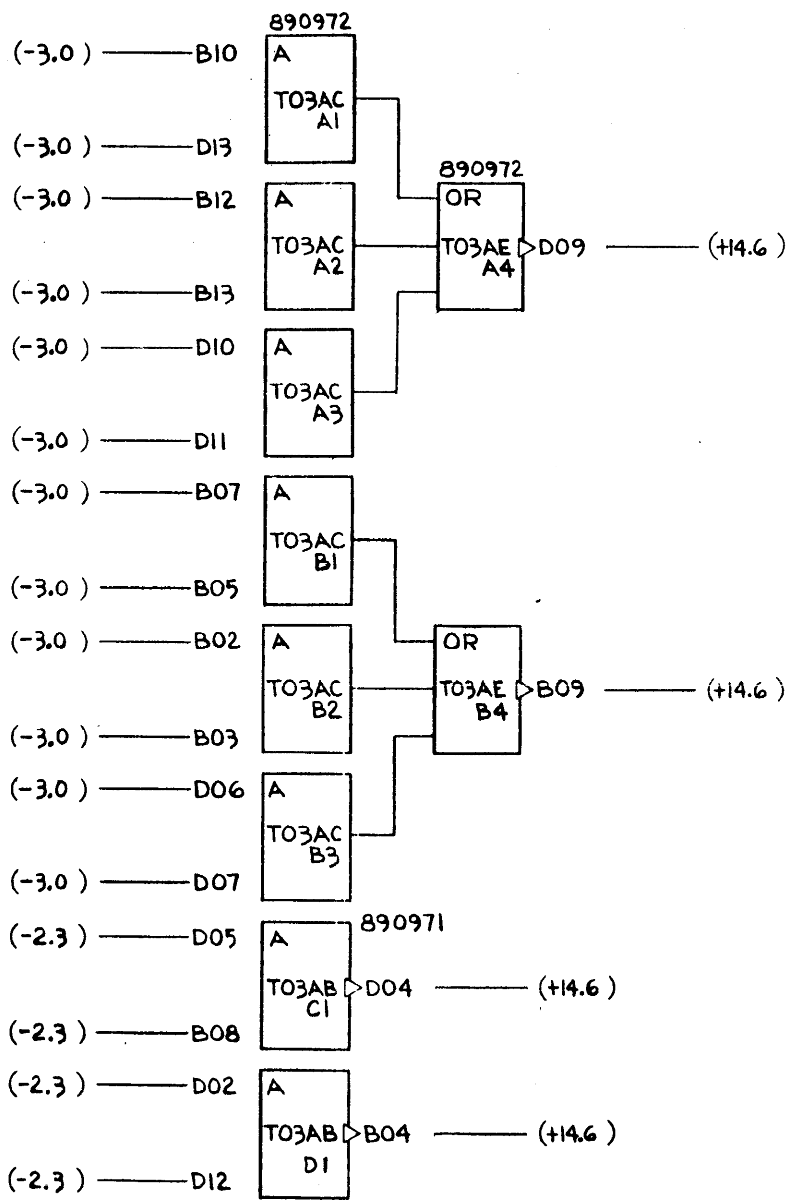


FIGURE 134

2-(3-2WAOI W/L) 2-2WAI W/L P/N 5800212

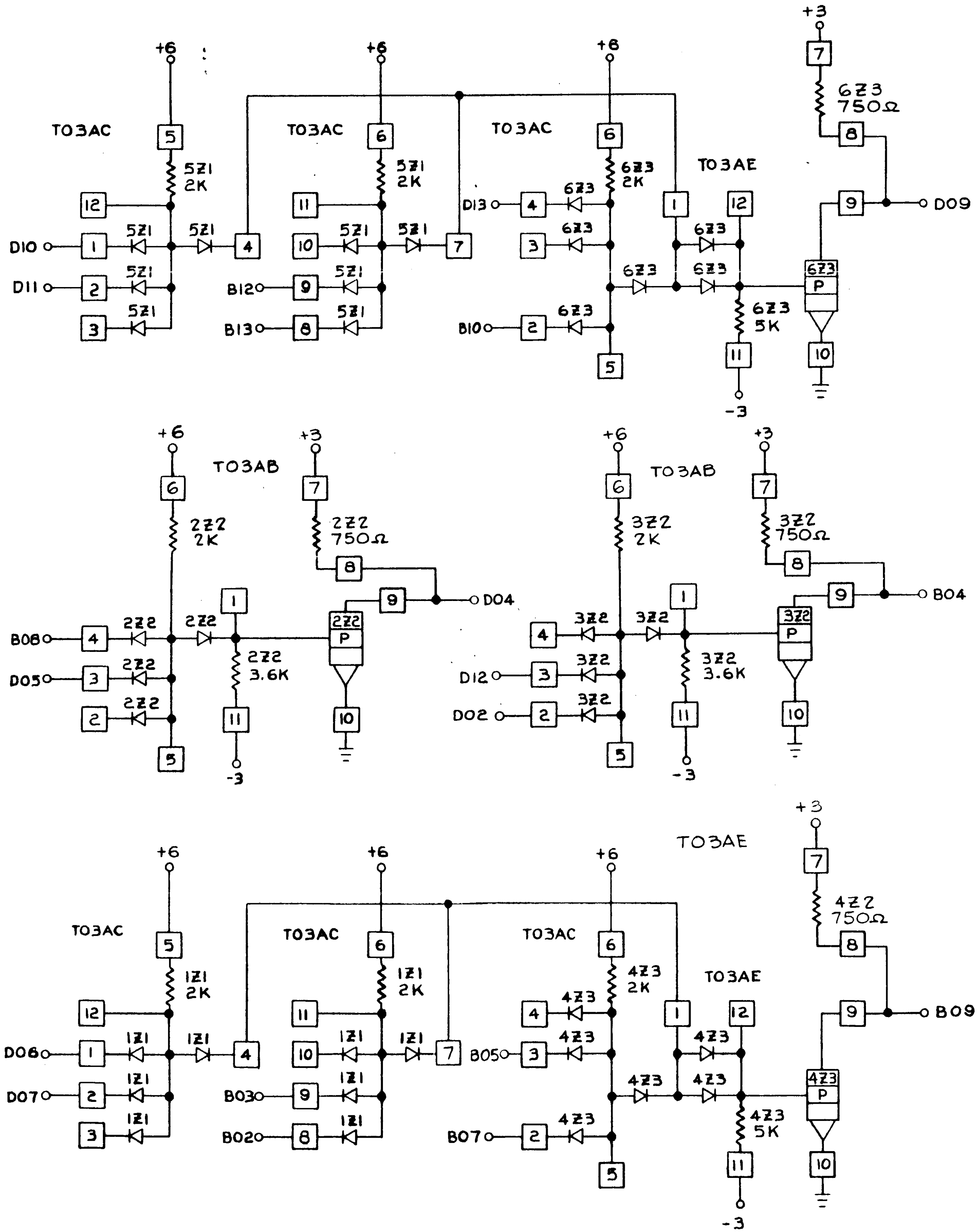


FIGURE 135

2-3WAI WO/L + 4-2WAI WO/L

PWR REQ

PIN	VOLT
D08	GRD
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800236	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	6

CARD TYPE	1-6

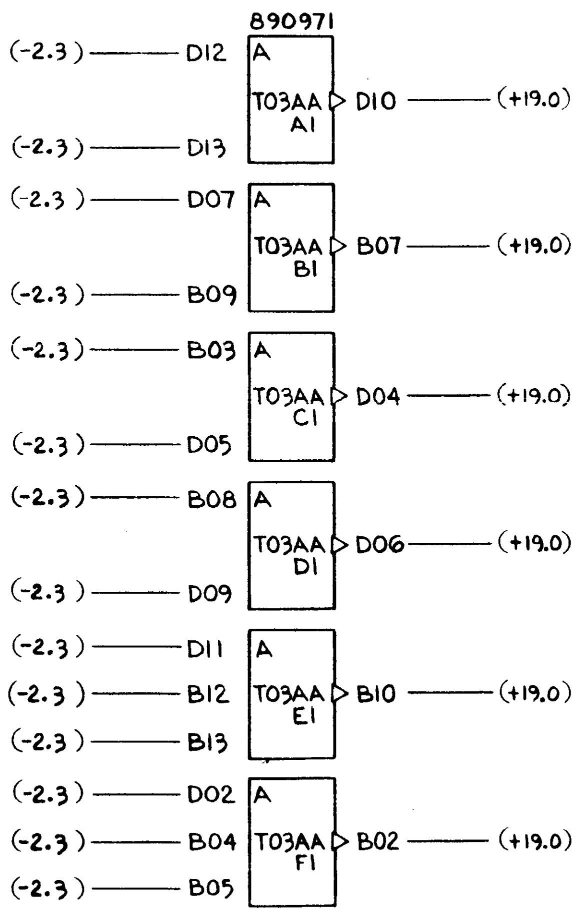


FIGURE 136

2-3WAI WO/L+4-2WAI WO/L   P/N 5800236

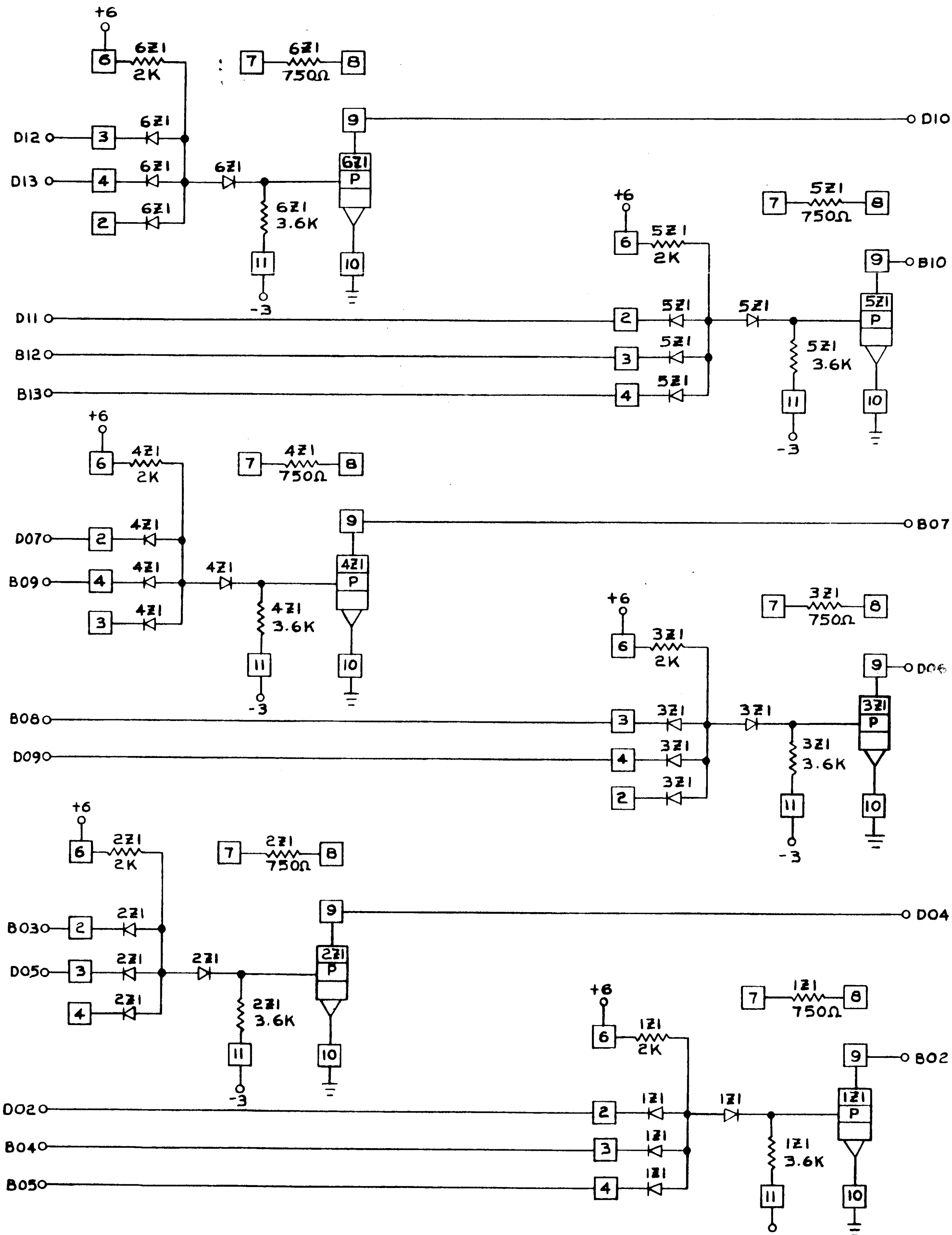


FIGURE 137

2-7WAI WO/L + 1-3WAI WO/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800244	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	3
FDD	361459	1

CARD TYPE	1-6

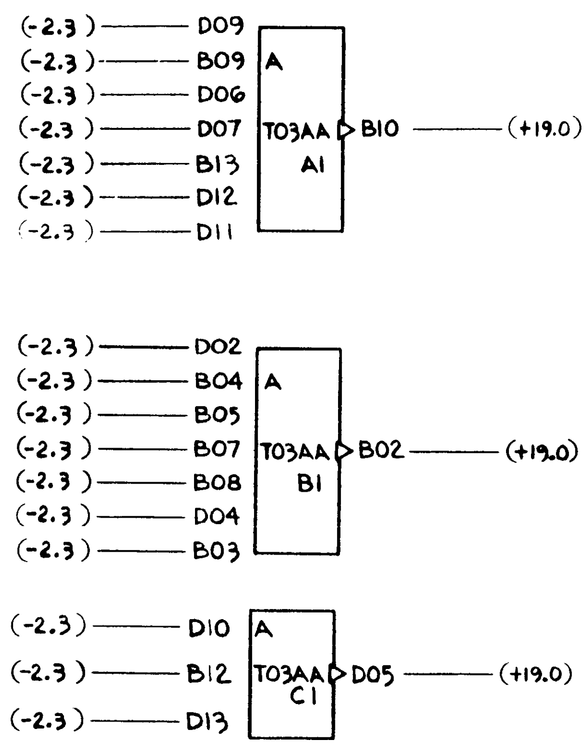
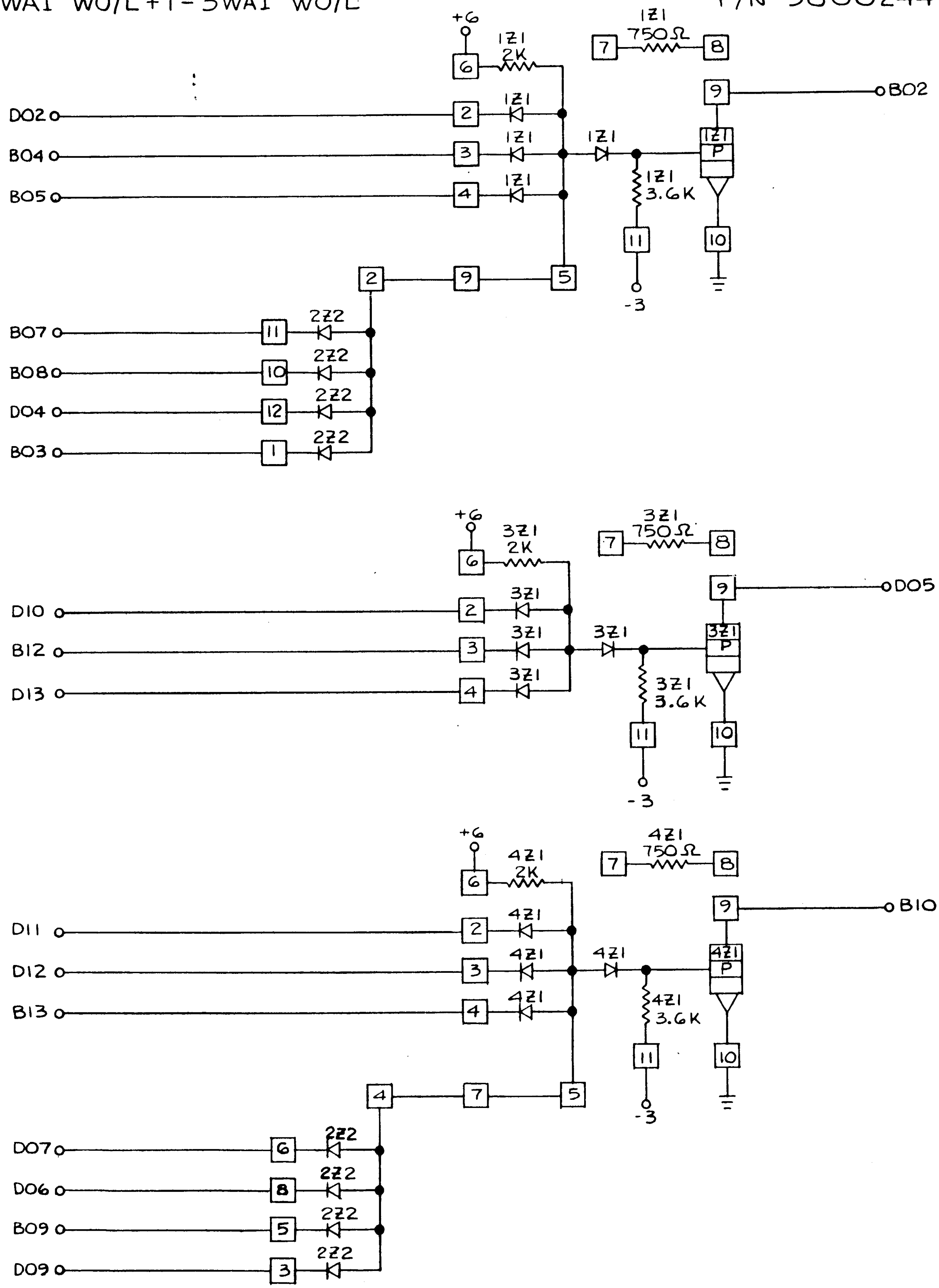


FIGURE 138



+6
1Z1
2K
1Z1
750Ω
DO2
BO4
BO5
BO7
BO8
DO4
BO3
BO2
3.6K
-3
2Z2
+6
3Z1
2K
750Ω
DO5
D10
B12
D13
3.6K
-3
+6
4Z1
2K
750Ω
B10
D11
D12
B13
3.6K
-3
DO7
DO6
BO9
DO9
2Z2

FIGURE 139

2-3WAPI W0/L + 4-2WAPI W0/L

PWR REQ

PIN	VOLT
D08	GRD
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800310	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	6

CARD TYPE	1-6

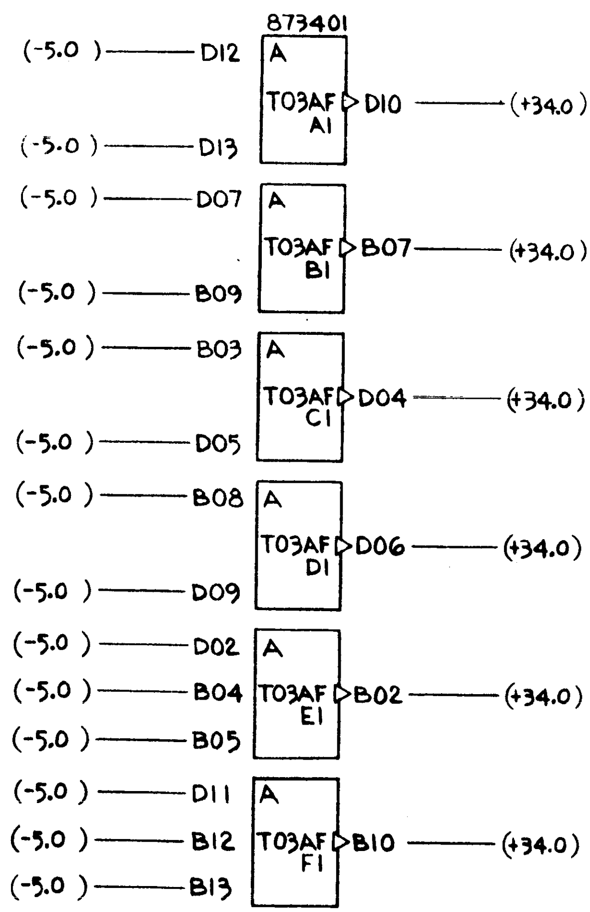


FIGURE 140

2-3WAPI WO/L+4-2WAPI WO/L P/N 5800310

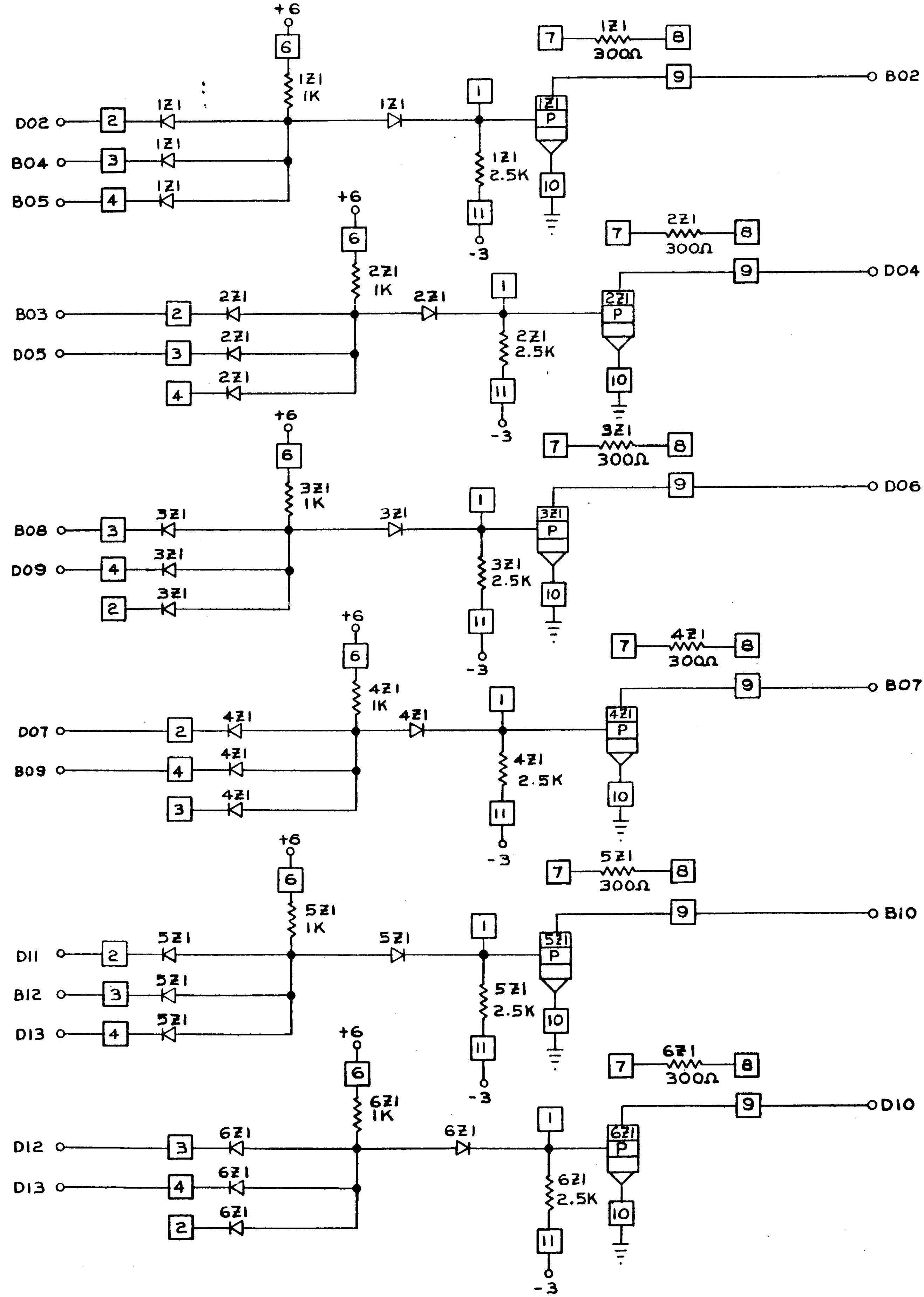


FIGURE 141

5-3WAPI WO/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5800311	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	5

CARD TYPE	1-6

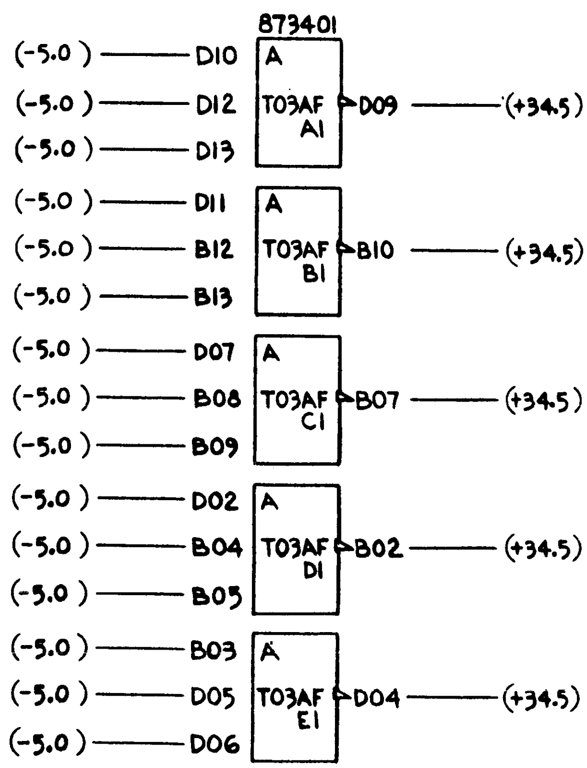


FIGURE 142

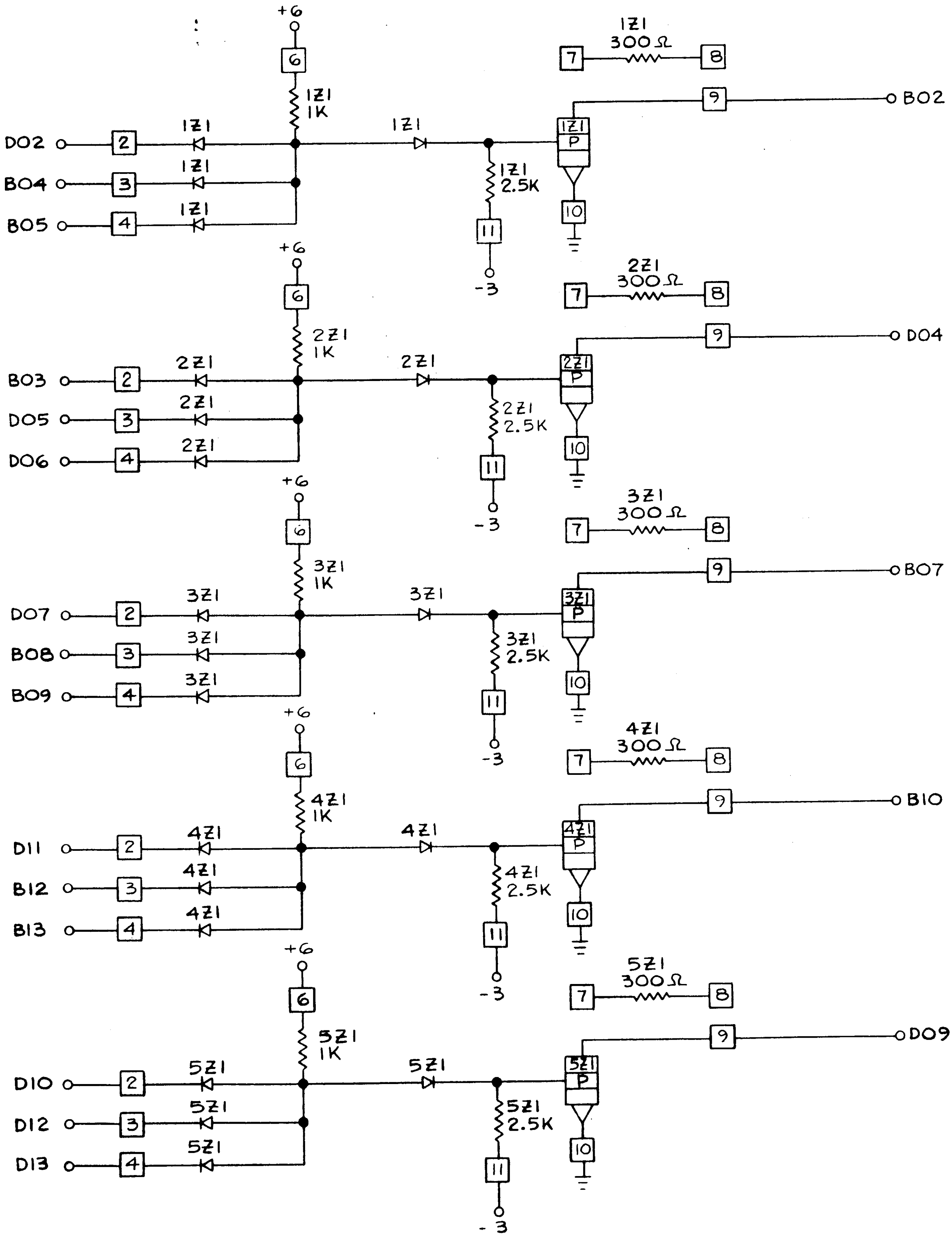

+6
6
1Z1
1K
D02
B04
B05
2
3
4
1Z1
1Z1
1Z1
1Z1
1Z1
2.5K
11
-3
1Z1
P
10
1Z1
300Ω
7
8
9
B02
+6
6
2Z1
1K
B03
D05
D06
2Z1
2Z1
2Z1
2Z1
2Z1
2.5K
-3
2Z1
300Ω
D04
+6
3Z1
1K
D07
B08
B09
3Z1
3Z1
3Z1
3Z1
3Z1
2.5K
-3
3Z1
300Ω
B07
+6
4Z1
1K
D11
B12
B13
4Z1
4Z1
4Z1
4Z1
4Z1
2.5K
-3
4Z1
300Ω
B10
+6
5Z1
1K
D10
D12
D13
5Z1
5Z1
5Z1
5Z1
5Z1
2.5K
-3
5Z1
300Ω
D09

FIGURE 143

6-2W EXCLUSIVE OR PI W/L

P/N5800428

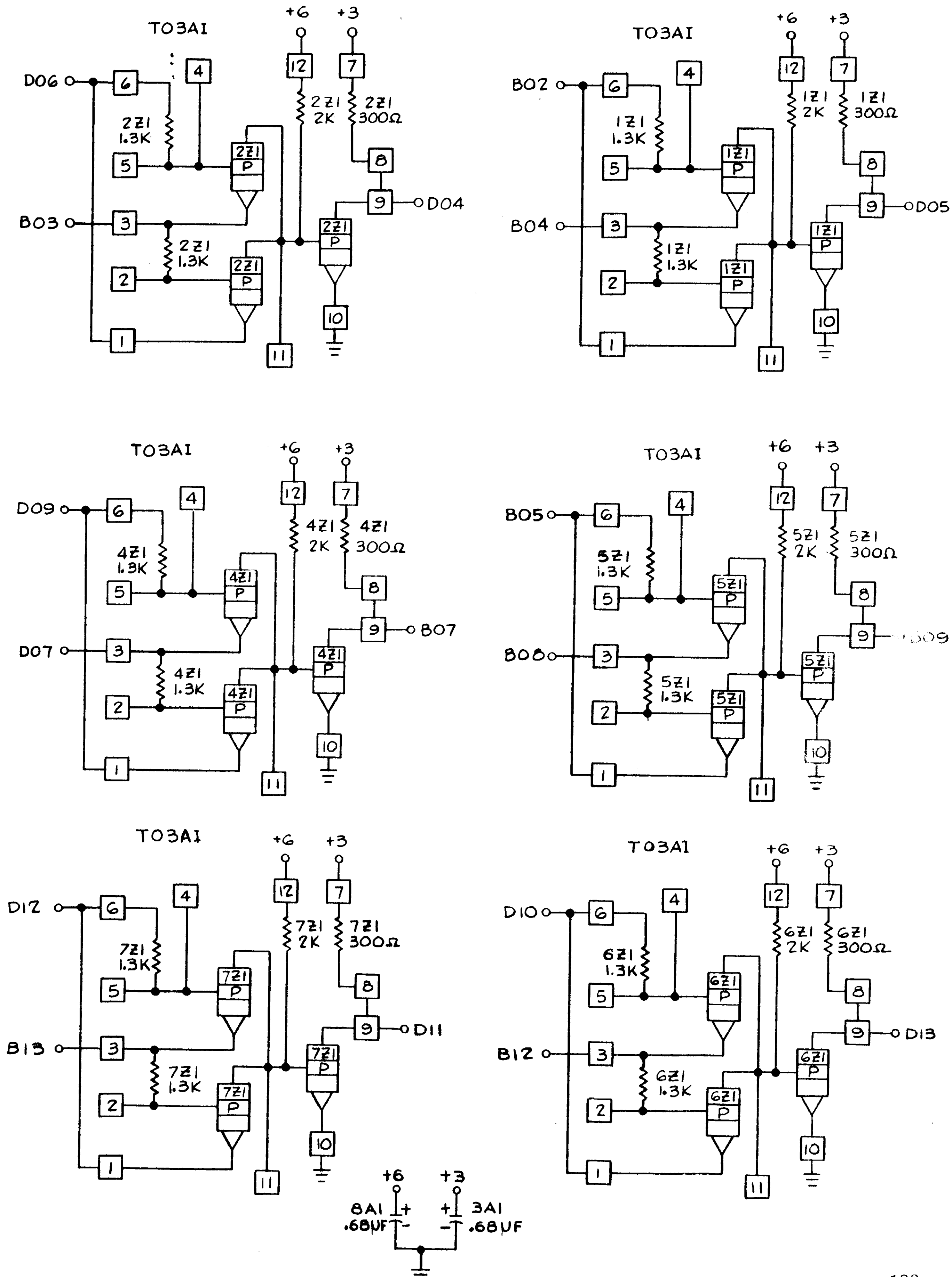


FIGURE 144

6- SEQUENCED-MULTIPLEX-LINE-DRIVERS

PWR REQ

PIN	VOLT
B11	+6
D03	+3
B06	-3
D08	GRD

SPECIAL APPLICATION NOTES

1. * B12, B13 SEQUENCED - +6V
2. Sequencing voltage should not change faster than .03 volts/nanosecond

P/N	5801664	
MODULE CODE	MODULE PART NUMBER	QTY
AOI	361453	6
T018	2414818	6
	2390306	12
	2414883	4

CARD TYPE	1-12

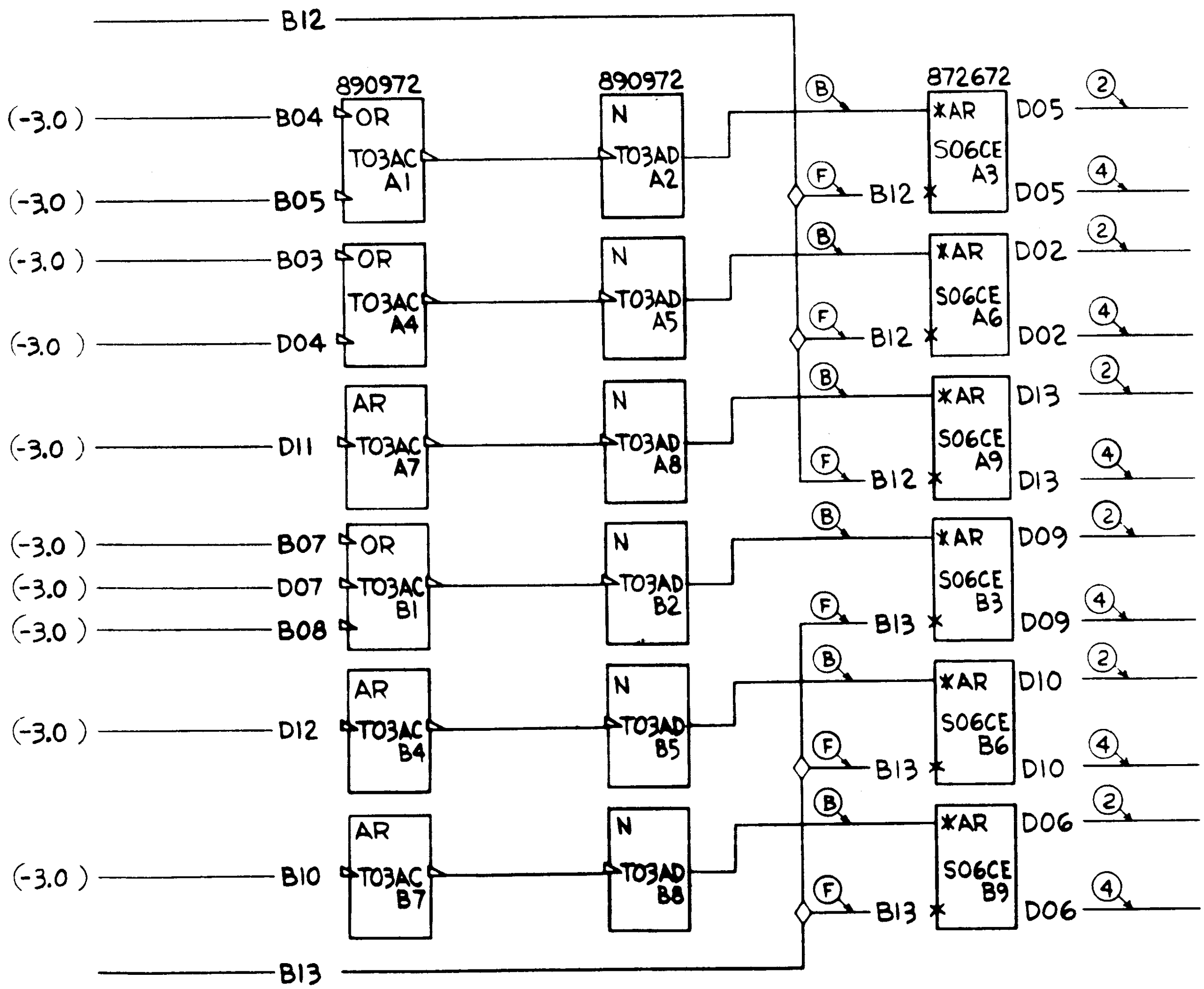


FIGURE 145

2-5WAI-W/PL+1-5WAI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B06	-3
B11	+6

SPECIAL APPLICATION NOTES

P/N	5803031	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	3
FDD	361459	1

CARD TYPE 1-6

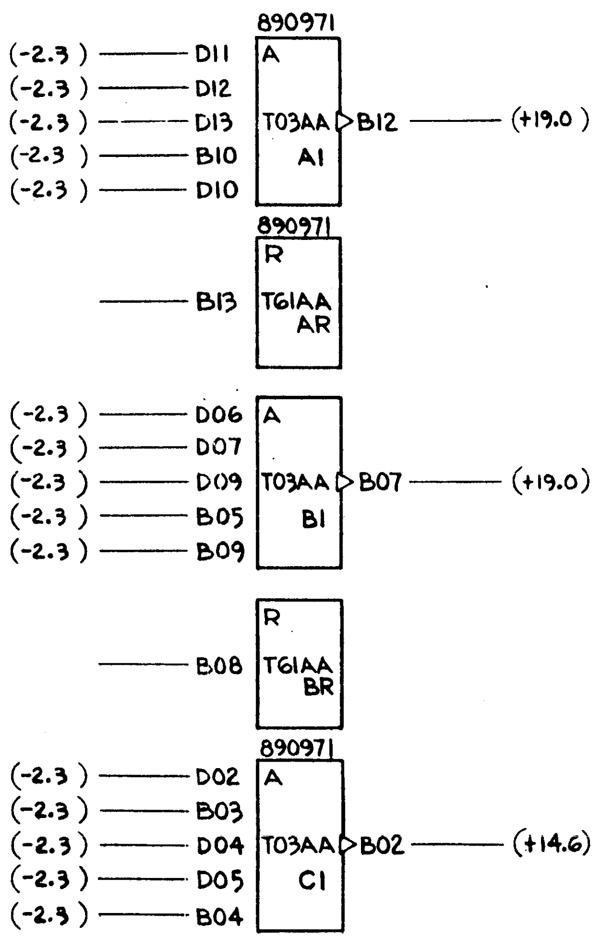


FIGURE 146

2-5WAI W/PL+1 - 5WAI W/L   P/N 5803031

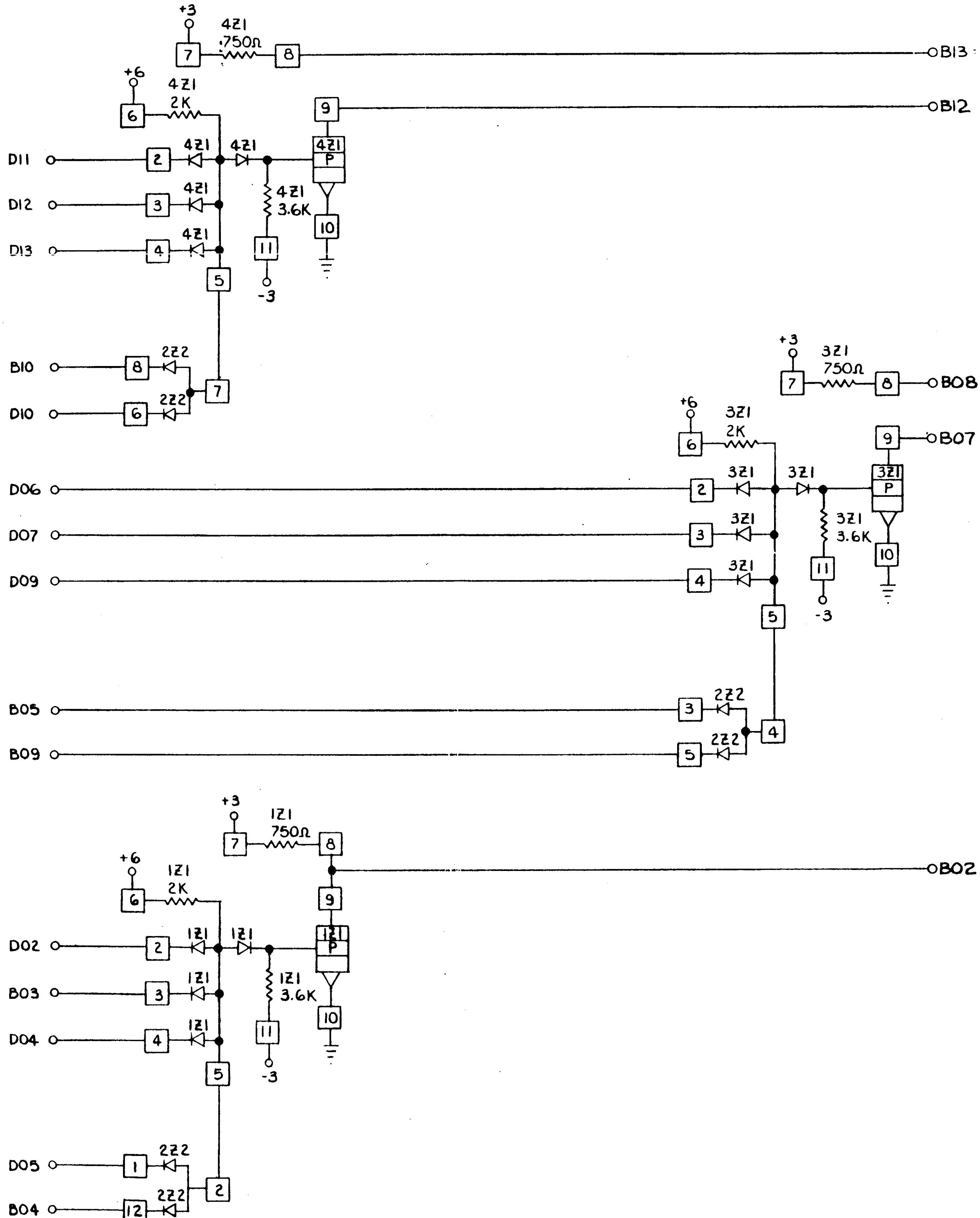


FIGURE 147

20 MULTIPLEX TERMINATOR RESISTORS TO +3V P/N 5803172

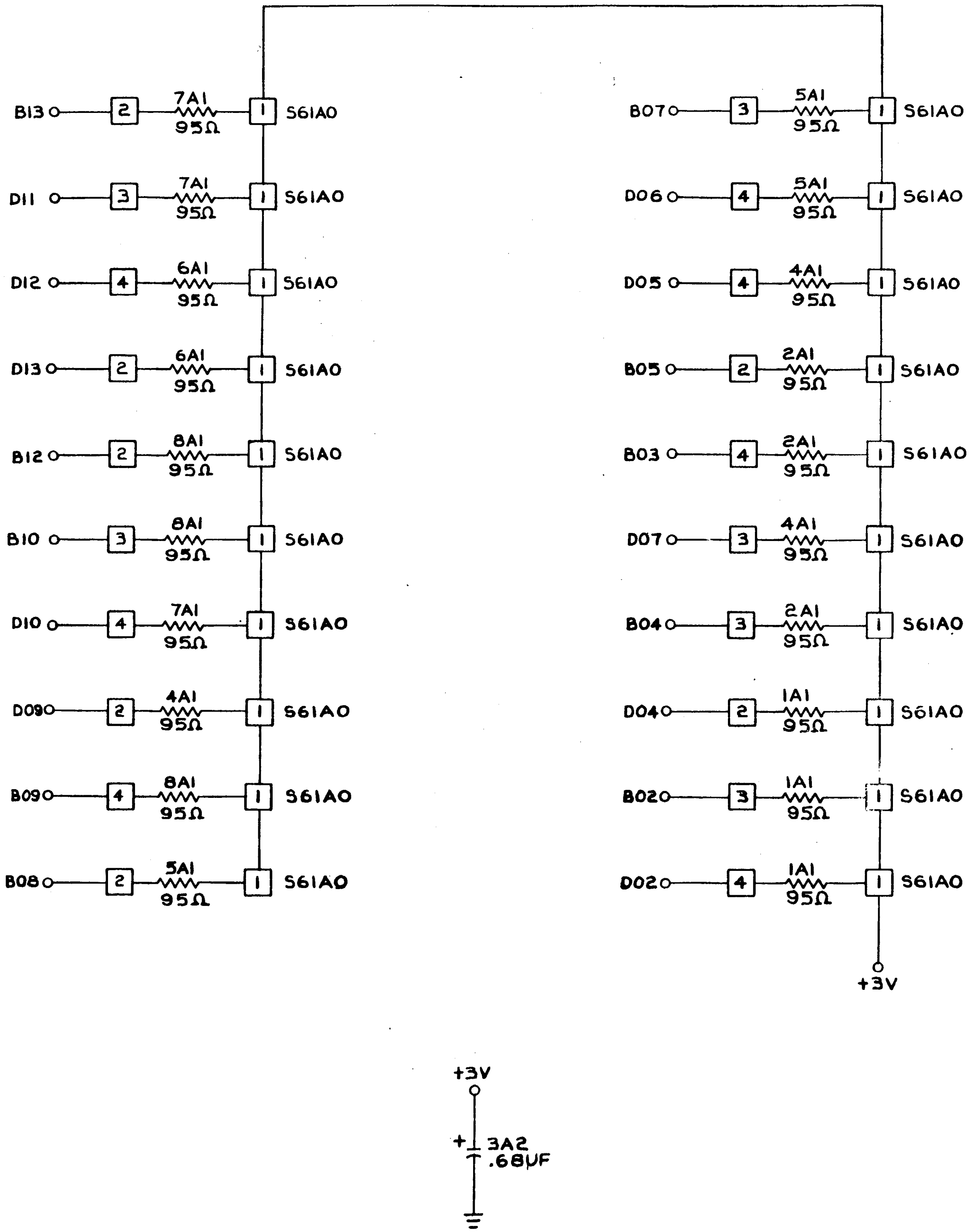


FIGURE 147A

6 GATED HIGH POWER DRIVERS

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5803309	
MODULE CODE	MODULE PART NUMBER	QTY
AOI	361453	6
HPD	361475	6
	2390445	2
	2414853	3

CARD TYPE	1-12

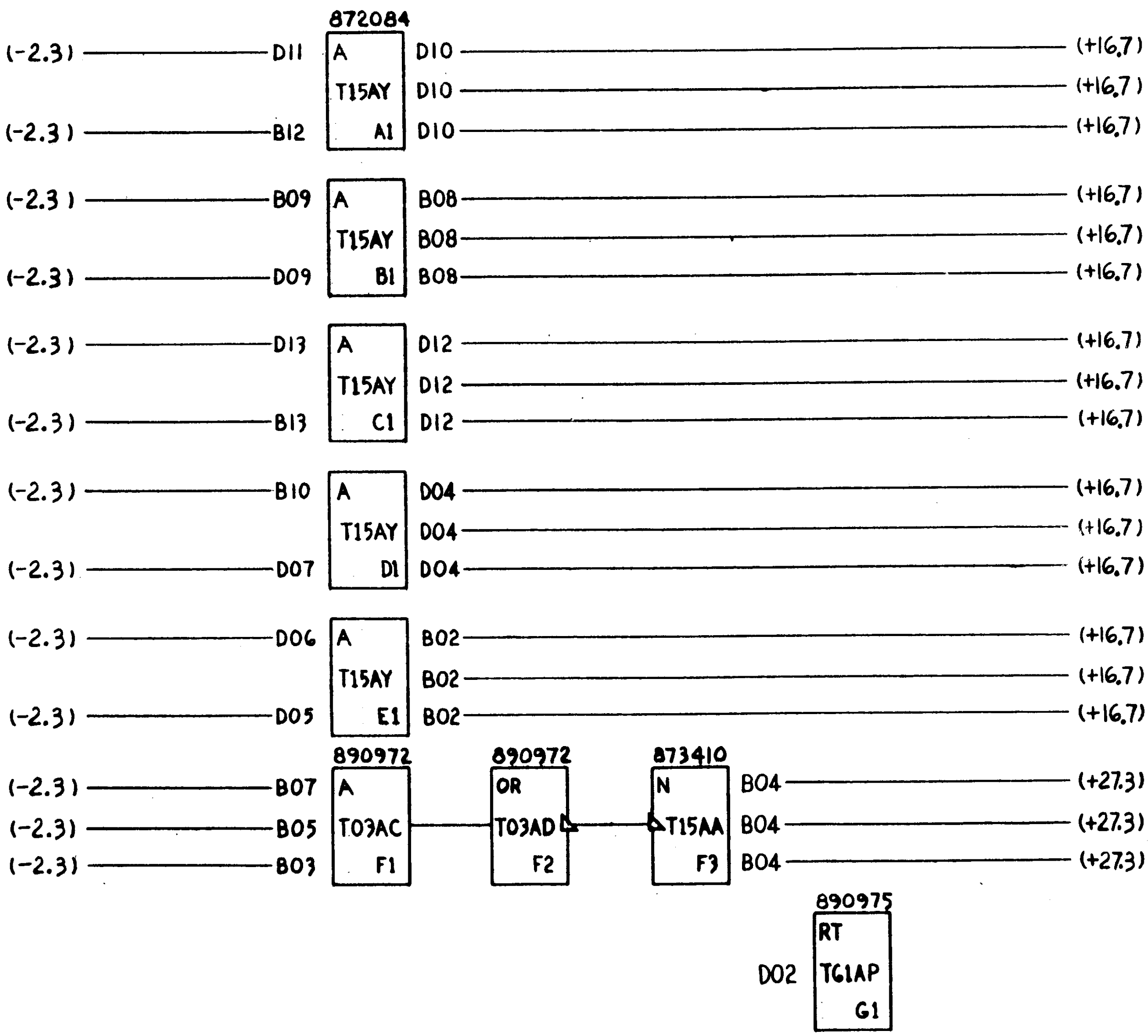


FIGURE 148

5-2WA HPD W/L + 1-3WA HPD W/L

P/N 5803309

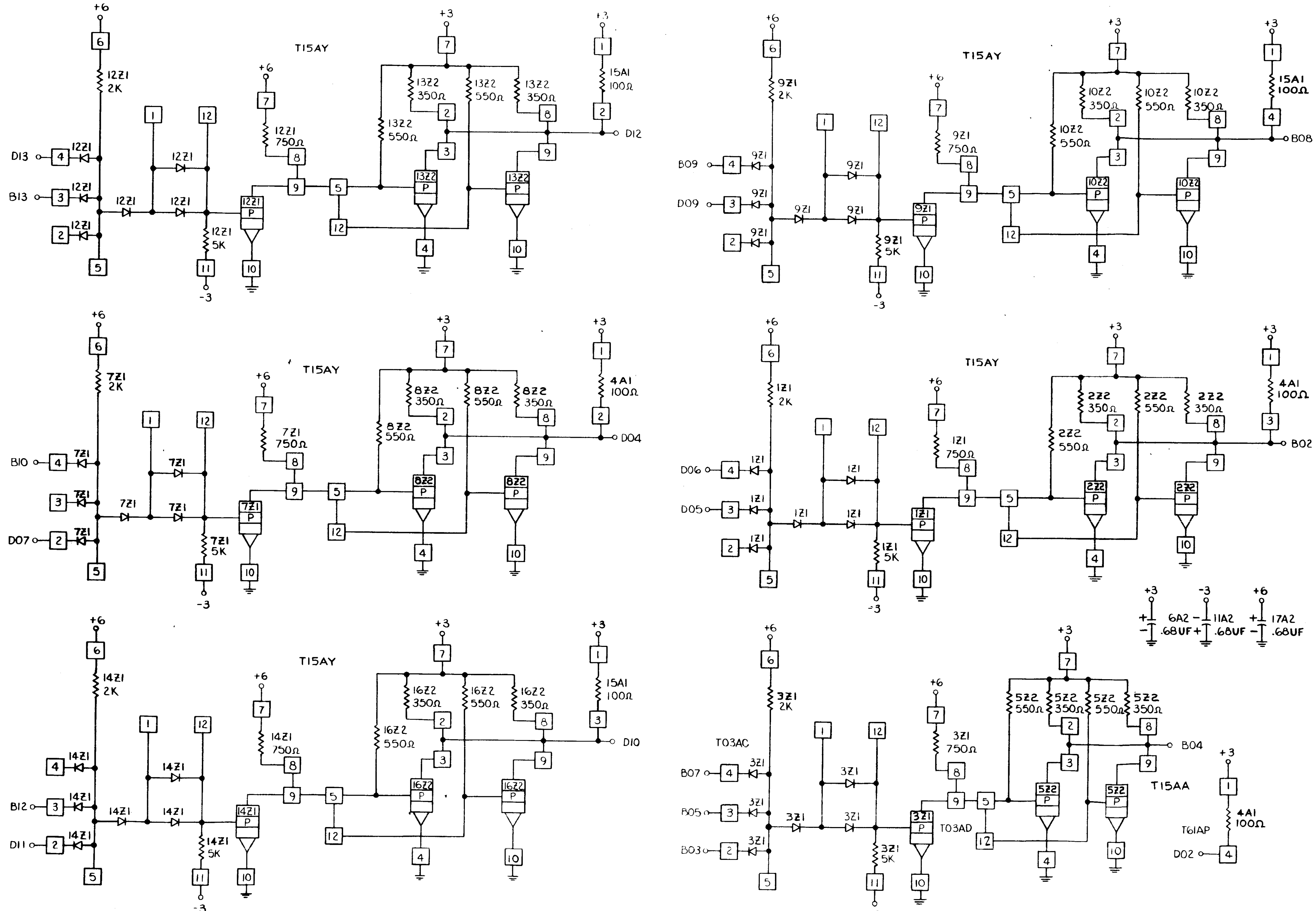


FIGURE 149

4-3WAI GATED COIL DRIVERS

PWR REQ

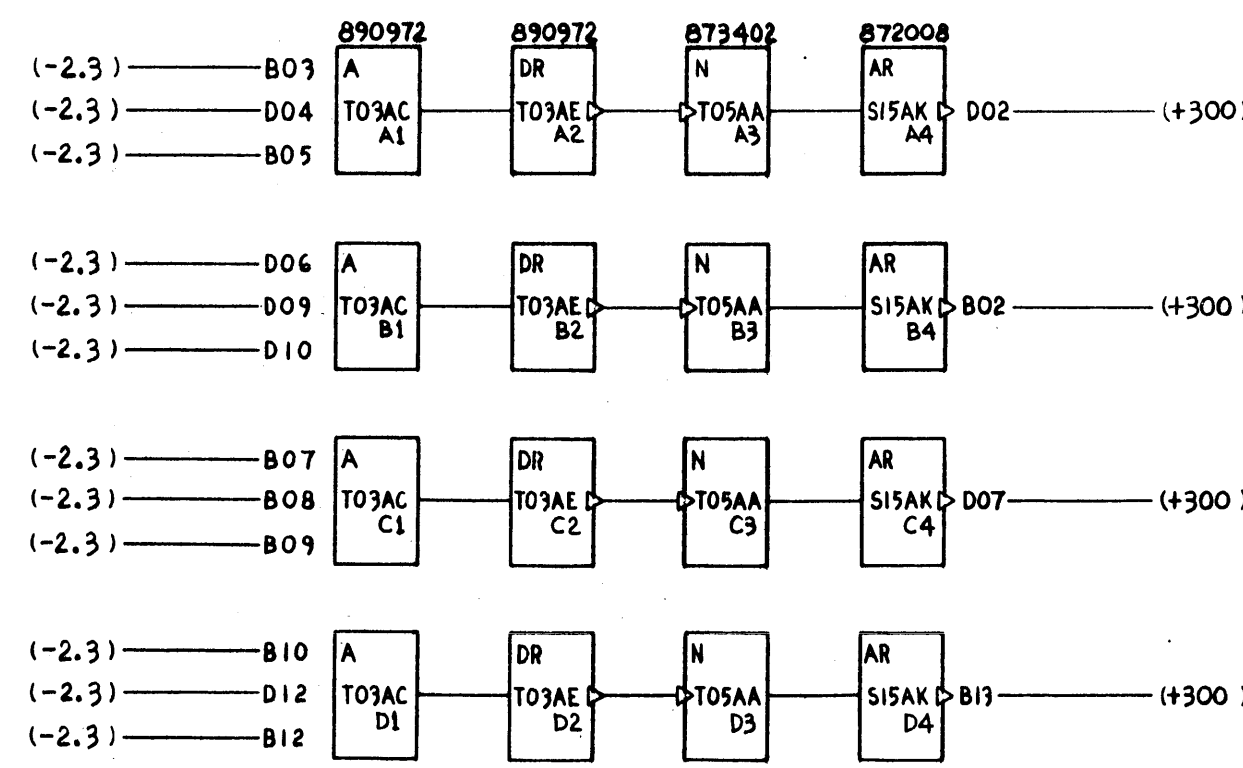
PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES :

P/N	5803332	
MODULE CODE	MODULE PART NUMBER	QTY
	369697	4
AOI	361453	4
DCI	361454	2
	2390419	2
	2414863	2
	611157	4

CARD TYPE	1-12

- Functional -



2-8 WAY EXCLUSIVE OR

P/N 5803394

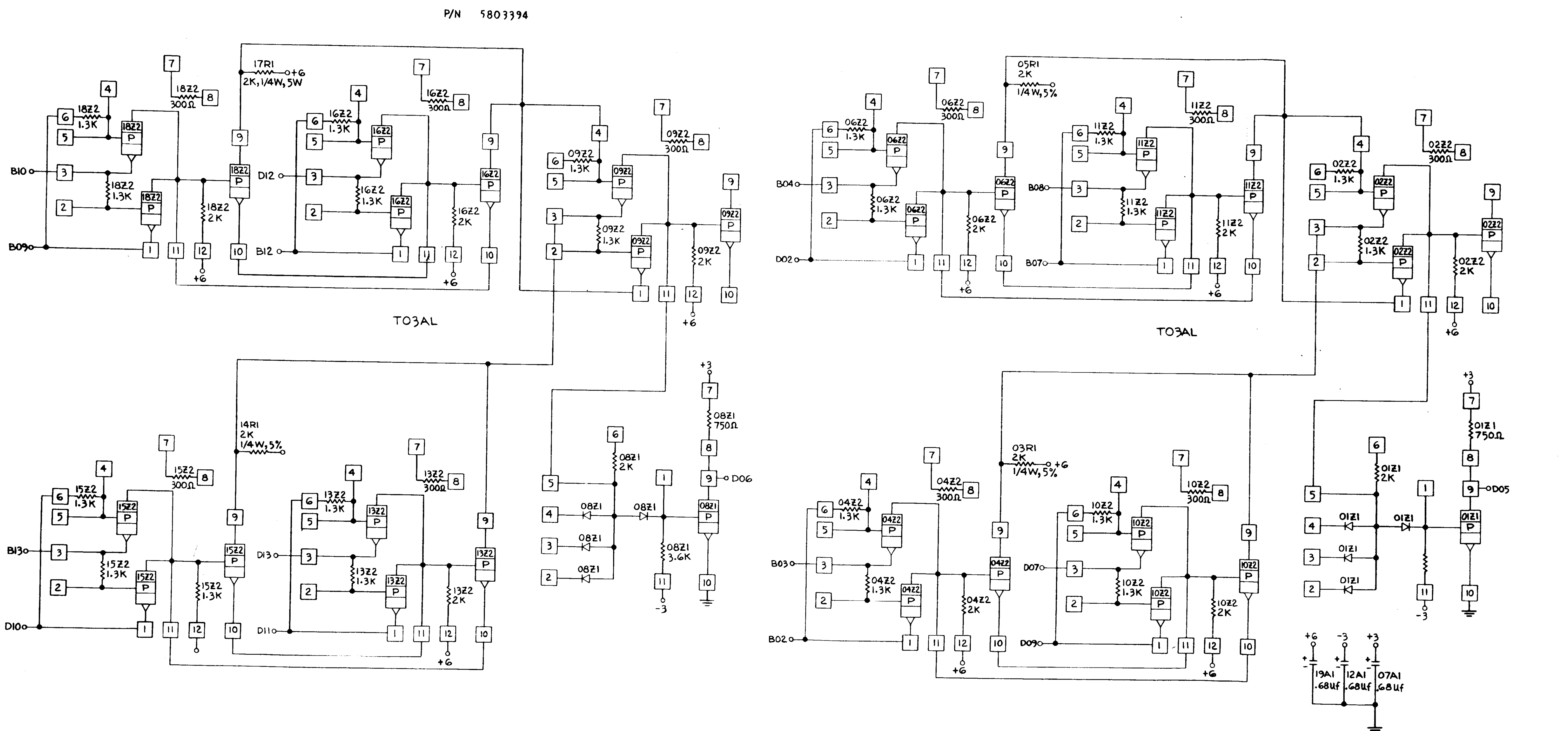


FIGURE 151

1-5WADI - W/L + 2-3WADI - W/L + 2-2WADCI - W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES
FUNCTIONAL

P/N	5803404	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	5
DCI	361454	3
FDD	361459	1
	2414883	3
	811308	1
	811300	24

CARD TYPE 1-12

- Functional -

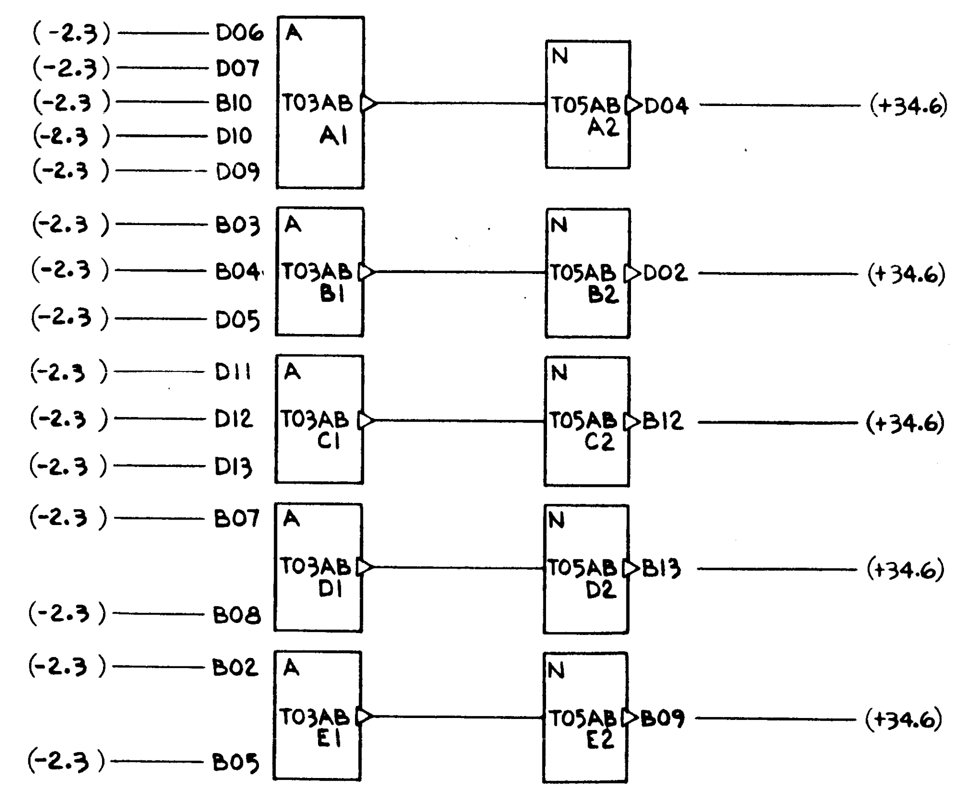


FIGURE 152

1-5WADI-W/L + 2-3WADI-W/L + 202WADCI-W/L

P/N 5803404

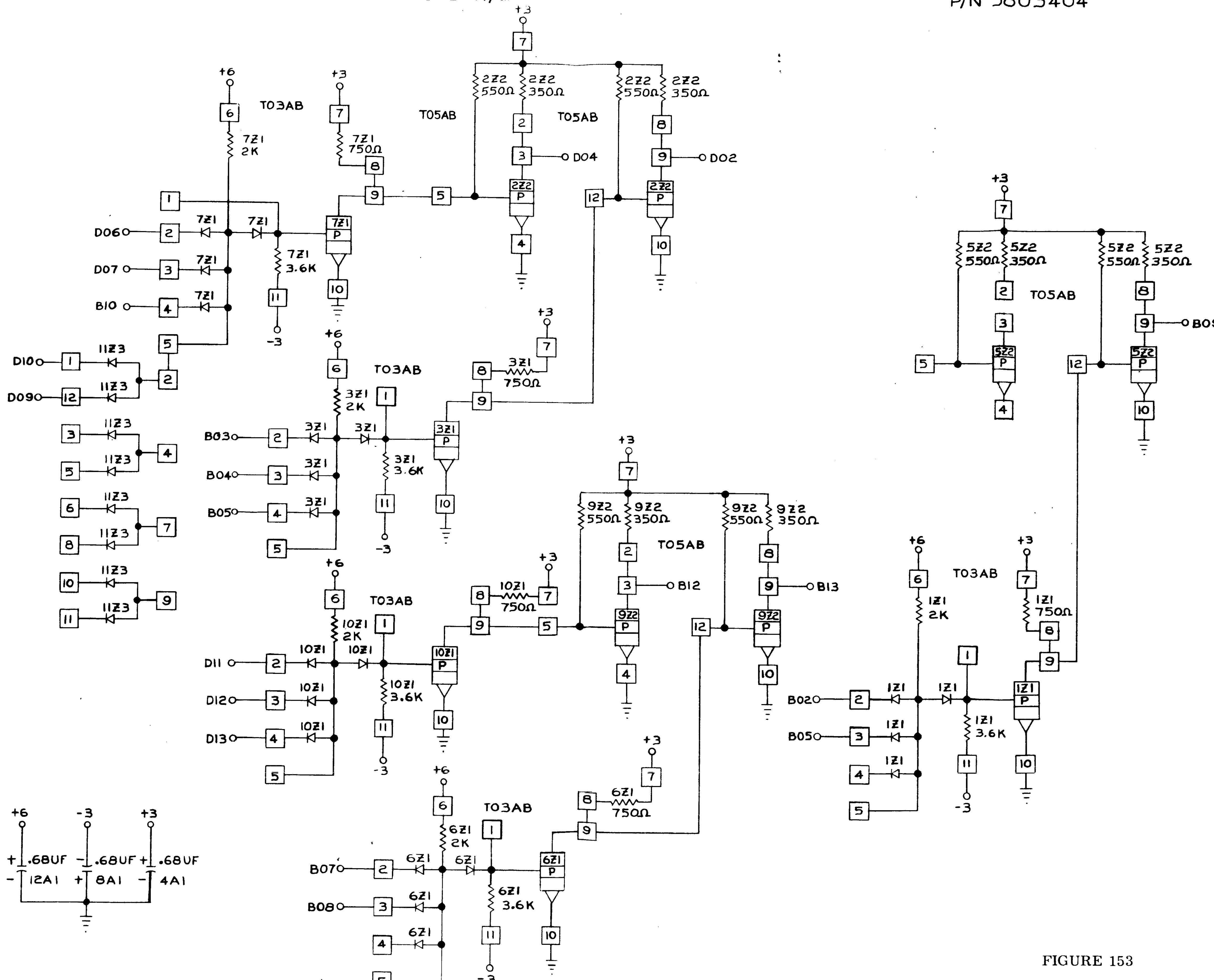


FIGURE 153

4-SINGLE LEG INPUT LATCHES + 1-IWAPI W/L

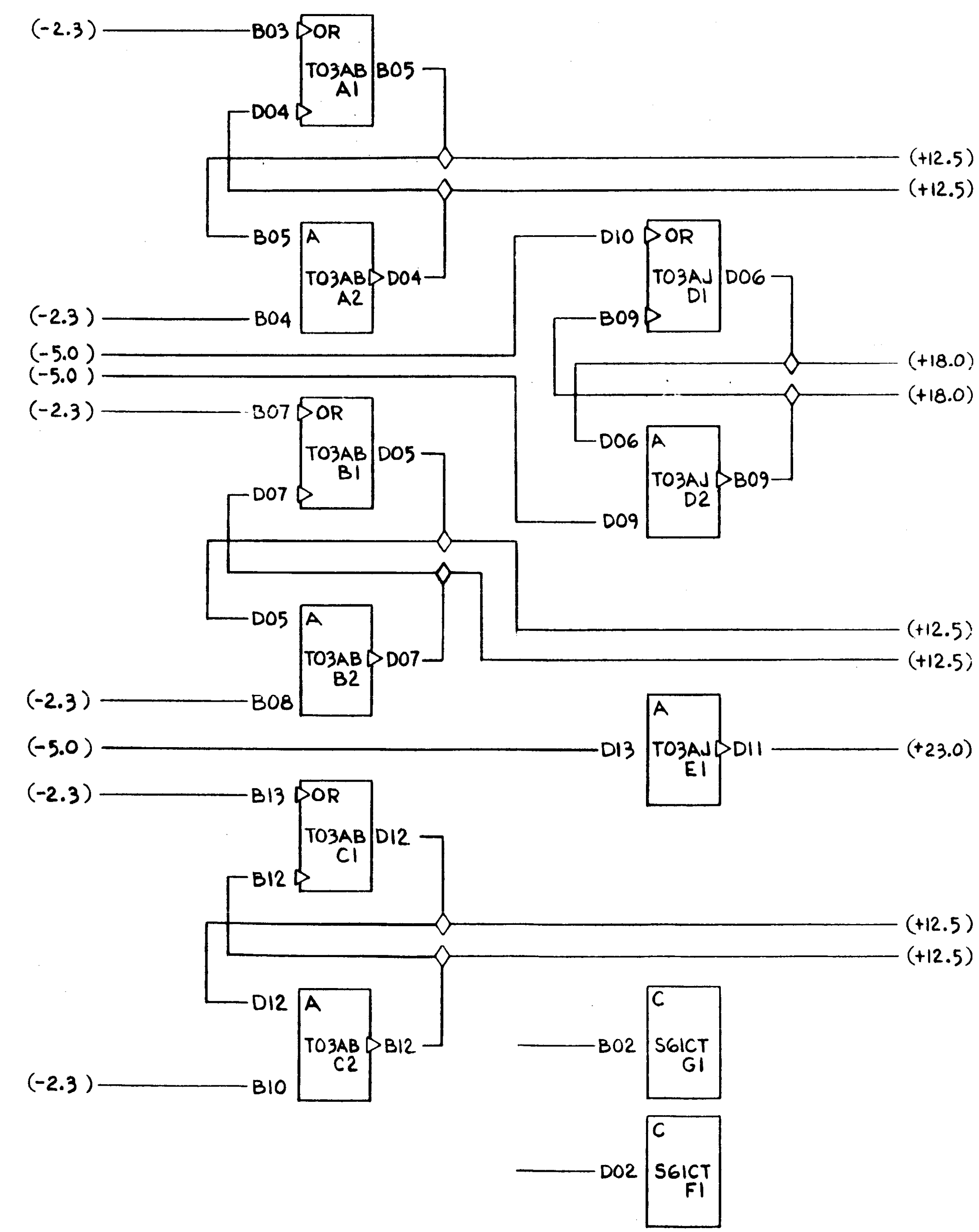
PWR REQ

PIN	VOLT
D08	GRD
D03	+ 3
B11	+ 6
B06	- 3

SPECIAL APPLICATION NOTES
Functional

P/N	5803405	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	6
API-3V	361473	3
	2390622	1
	2414883	3

CARD TYPE	1-12



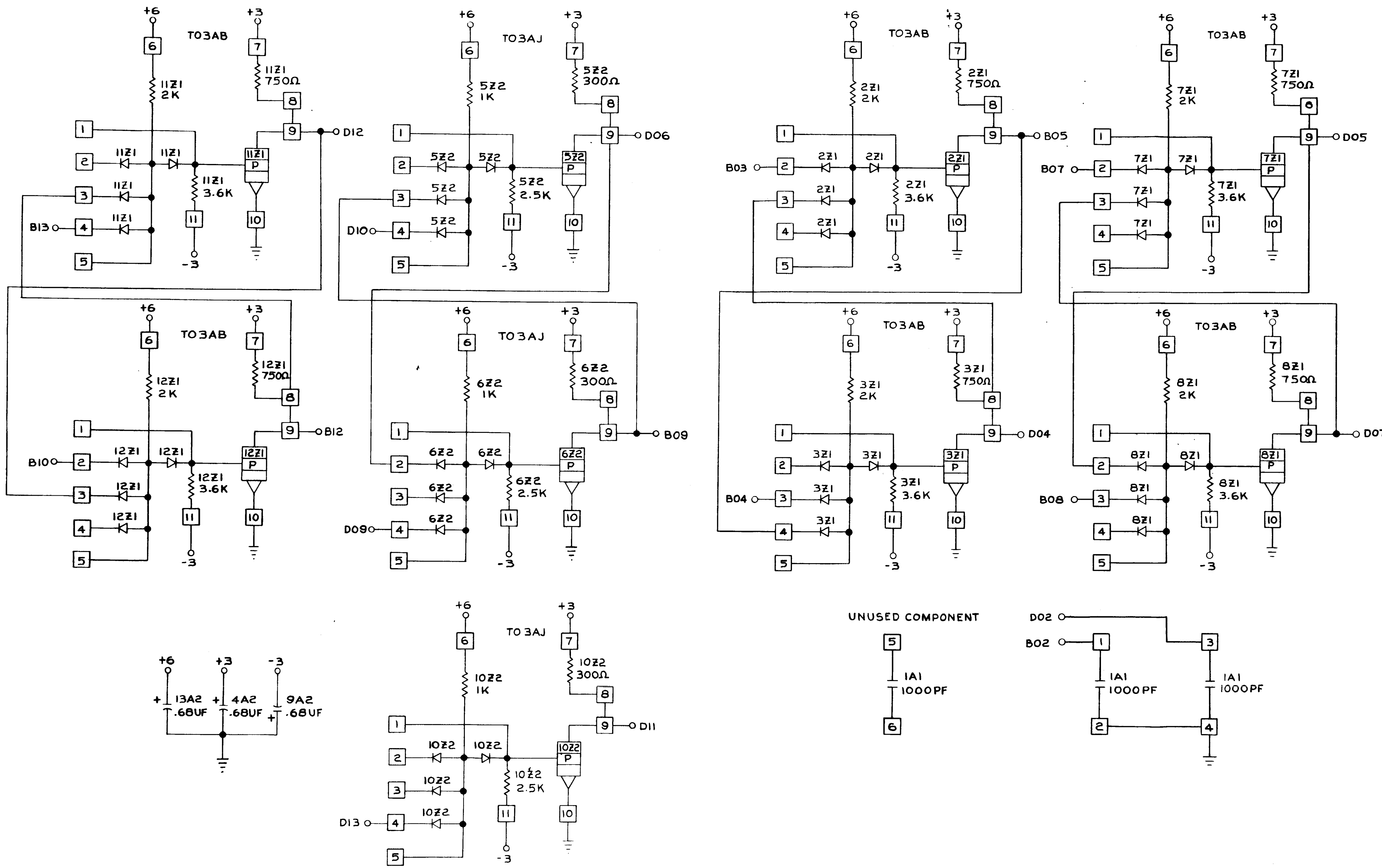

+6
+3
-3
TO3AB
TO3AJ
11Z1 2K
11Z1 750Ω
11Z1 3.6K
12Z1 2K
12Z1 750Ω
12Z1 3.6K
5Z2 1K
5Z2 300Ω
5Z2 2.5K
6Z2 1K
6Z2 300Ω
6Z2 2.5K
2Z1 2K
2Z1 750Ω
2Z1 3.6K
3Z1 2K
3Z1 750Ω
3Z1 3.6K
7Z1 2K
7Z1 750Ω
7Z1 3.6K
8Z1 2K
8Z1 750Ω
8Z1 3.6K
10Z2 1K
10Z2 300Ω
10Z2 2.5K
D12
B13
B12
B10
D06
D10
B09
D09
B05
B03
D04
B04
D05
B07
D07
B08
D11
D13
13A2 .68UF
4A2 .68UF
9A2 .68UF
UNUSED COMPONENT
1A1 1000PF
D02
B02

FIGURE 155

10-1WAI W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5803421	
MODULE CODE	MODULE PART NUMBER	QTY
AI	361451	10
	2414893	3

CARD TYPE	1-12

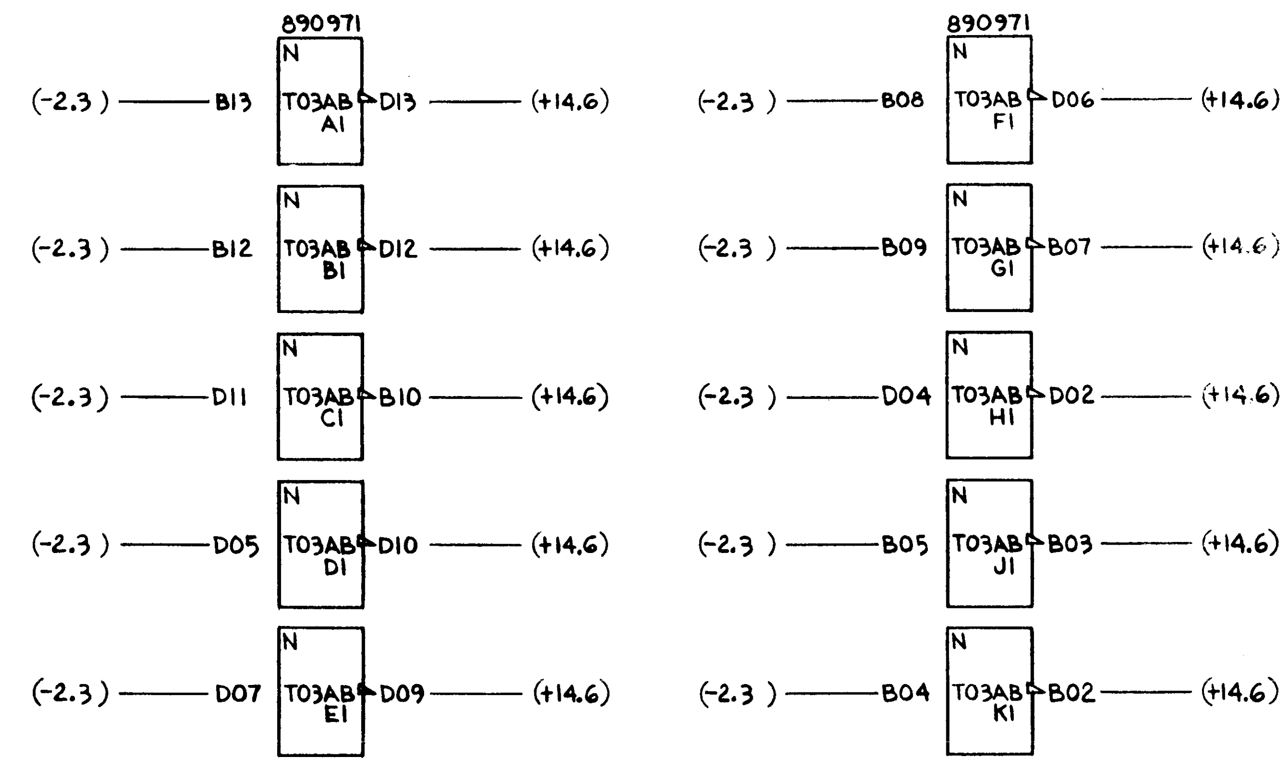


FIGURE 156

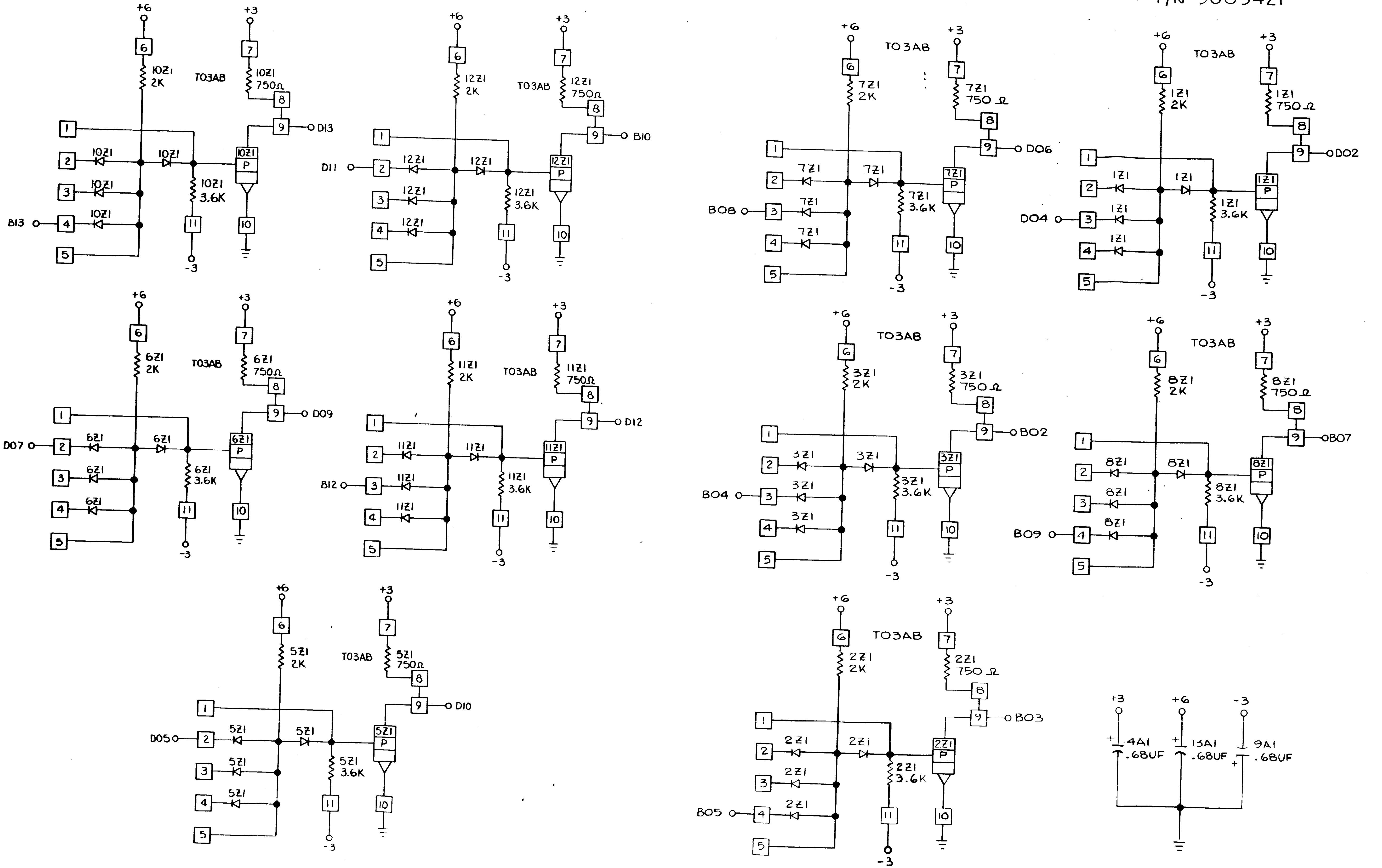

T03AB
D13
B13
D11
B10
D06
B08
D02
D04
D09
D07
D12
B12
B02
B04
B07
B09
D10
D05
B03
B05
4A1 .68UF
13A1 .68UF
9A1 .68UF

FIGURE 157

10 API WO/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

:

P/N	5803447	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	10
	2414883	2

CARD TYPE	1-12

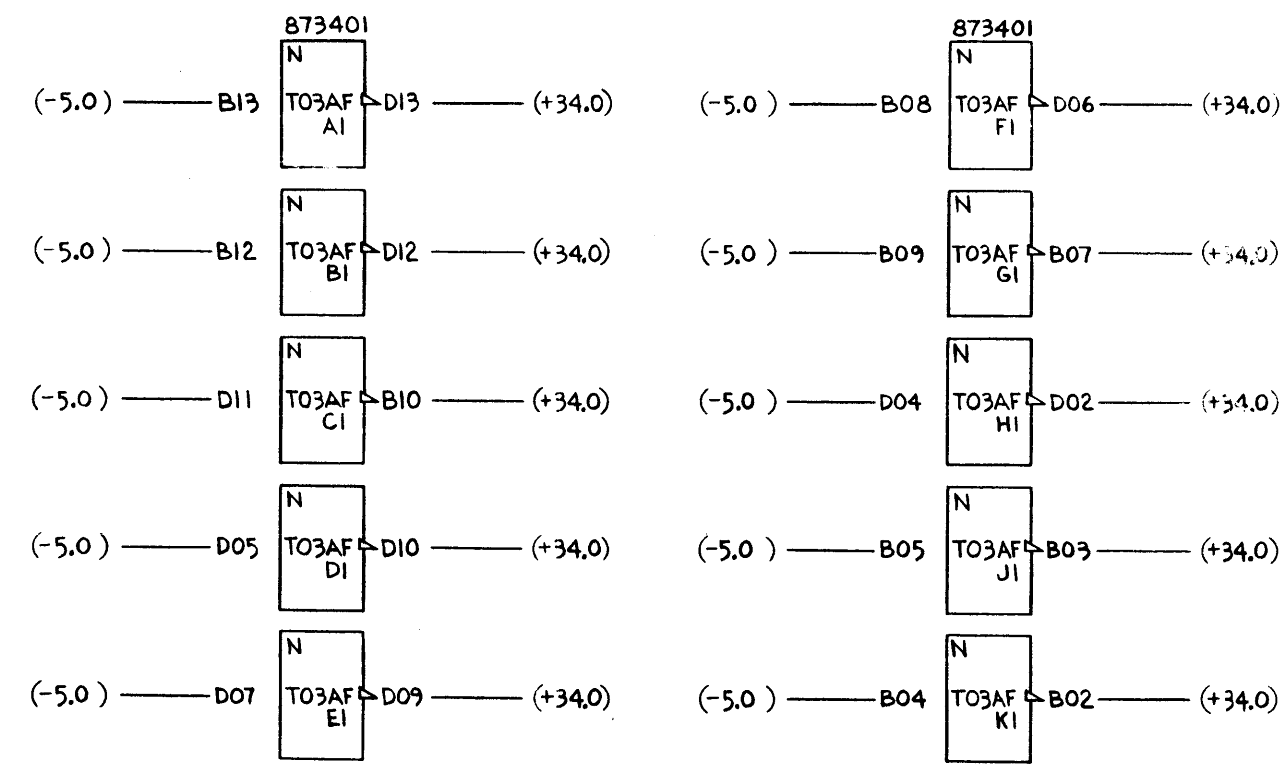


FIGURE 158

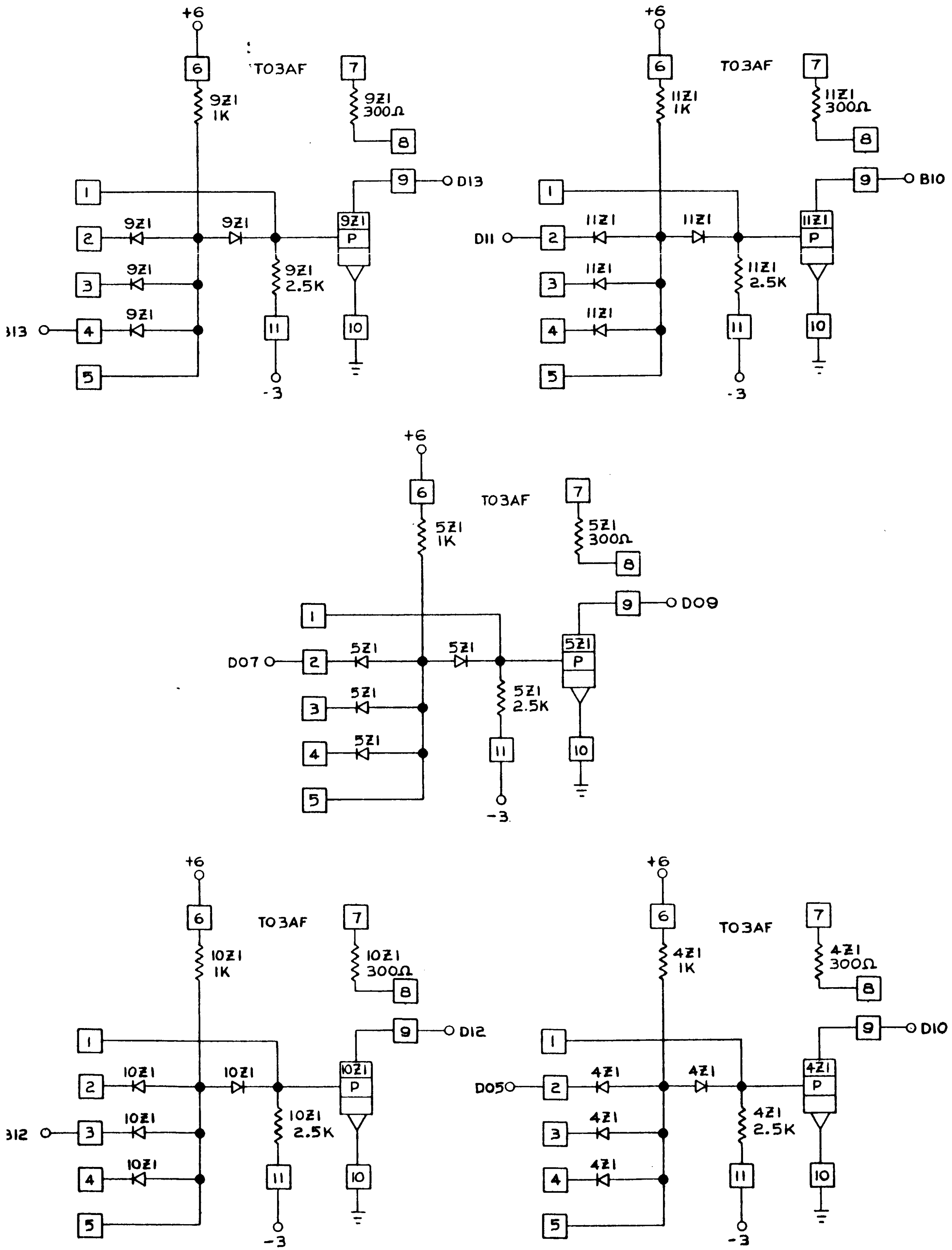

+6
TO3AF
9Z1 1K
9Z1 300Ω
9Z1 2.5K
9Z1
P
D13
B13
-3
11Z1 1K
11Z1 300Ω
11Z1 2.5K
11Z1
B10
D11
5Z1 1K
5Z1 300Ω
5Z1 2.5K
5Z1
D09
D07
10Z1 1K
10Z1 300Ω
10Z1 2.5K
10Z1
D12
B12
4Z1 1K
4Z1 300Ω
4Z1 2.5K
4Z1
D10
D05

FIGURE 159

2-VARIABLE SINGLE SHOTS

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES:

TABLE OF OUTPUT PULSE WIDTH AND RECOVERY TIME

C_T	T_{MAX}	T_{MIN}	TR_{MIN}
100 PF	207 NS	78 NS	92 NS
300 PF	620 NS	234 NS	276 NS
0.001 UF	2.07 US	780 NS	920 NS
0.0033 UF	6.85 US	2.57 US	3.04 US
0.01 UF	20.7 US	7.8 US	9.2 US
0.33 UF	68.5 US	25.7 US	30.4 US
0.1 UF	207 US	78 US	92 US
0.33 UF	685 US	257 US	304 US
1.0 UF	2.07 MS	780 US	920 US
3.3 UF	6.85 MS	2.57 MS	3.04 MS
10 UF	20.7 MS	7.8 MS	9.2 MS
27 UF	56.0 MS	21.0 MS	25 MS

P/N 5803617

MODULE CODE	MODULE PART NUMBER	QTY
	483119	2
	491009	2
	492441	1
	491263	1
	217079	1
AI	361451	2
AOI	361453	2
II	361479	1
DCI	361454	1
FDD	361459	1
	2414883	3
	2390202	2
	2390527	1

CARD TYPE 1-12

Functional

WHEN USING VALUES OF C_T OTHER THAN THE ABOVE, USE THE FOLLOWING FORMULA:

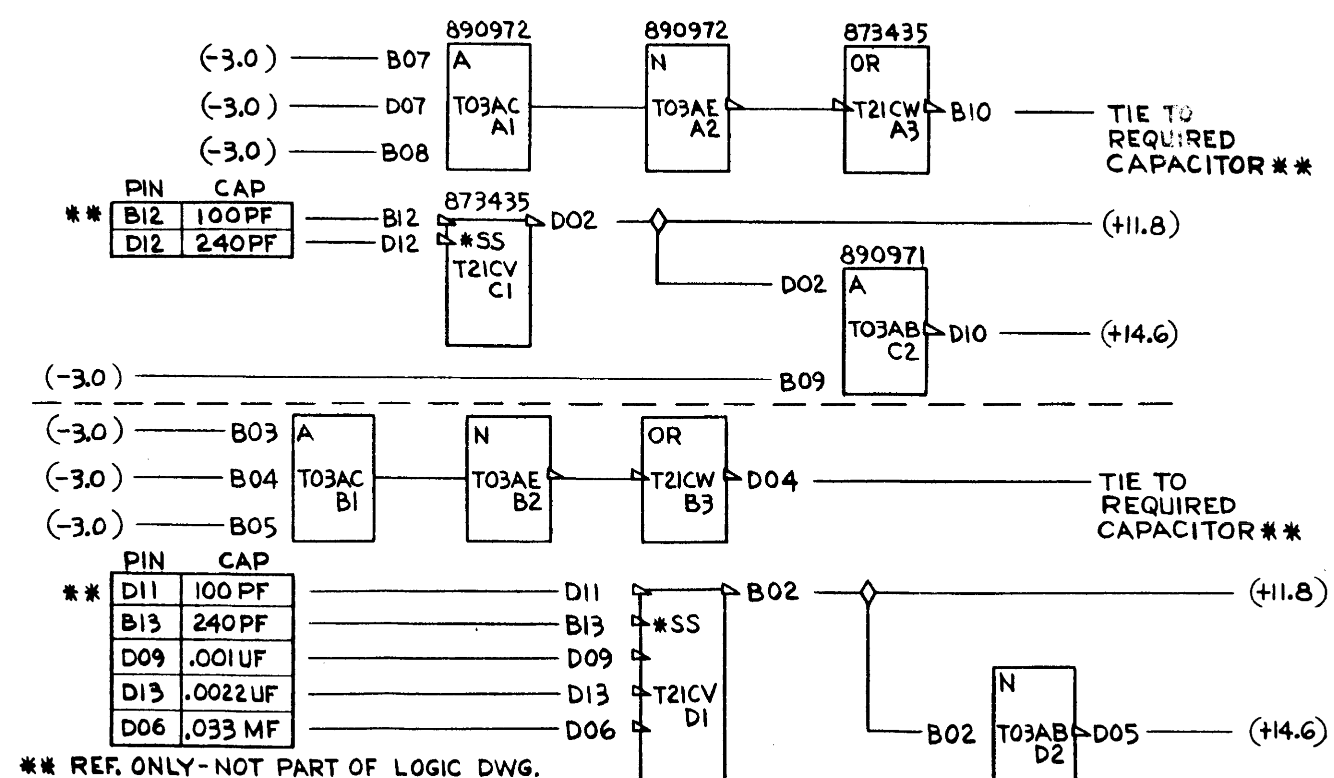
$T_{MAX} = 2.07 \times 10^3 \, C_T$ SEC

$T_{MIN} = 0.78 \times 10^3 \, C_T$ SEC

$TR_{MIN} = 0.92 \times 10^3 \, C_T$ SEC

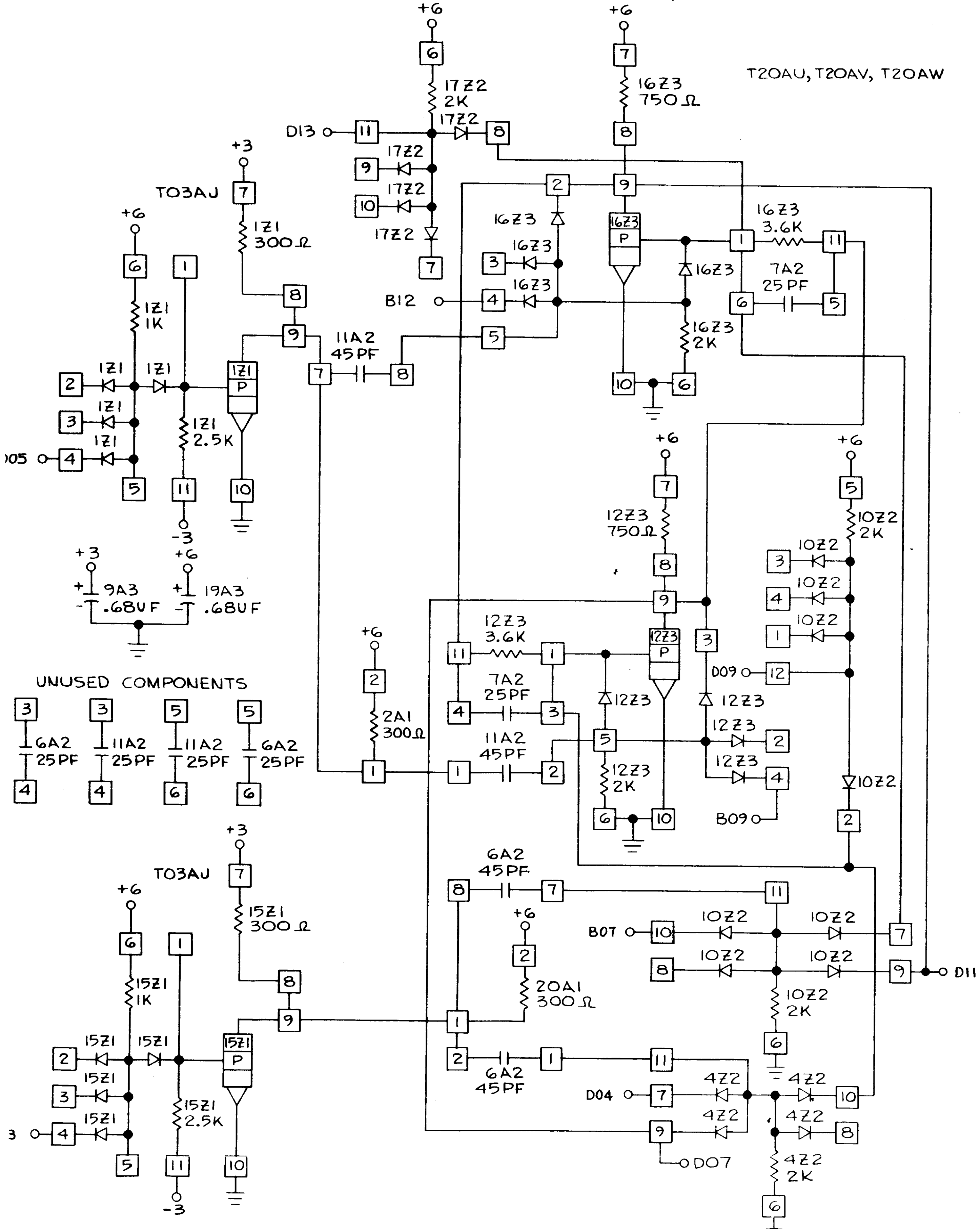
(C_T HAS UNITS OF FARADS)

THE SSB IS TRIGGERED ON BY A NEGATIVE GOING PULSE, HAVING A TRANSITION NO GREATER THAN 50 NANOSECONDS AND A WIDTH NO LESS THAN 30 NANOSECONDS. UPON TRIGGERING, THE OUTPUT DROPS TO SATURATION LEVEL FOR THE PRE-SET DURATION BEFORE RETURNING TO THE 3V LEVEL AGAIN. A MINIMUM RECOVERY TIME FOR THE CAPACITOR IS REQUIRED BEFORE THE NEXT TRIGGER PULSE CAN BE APPLIED. IF THE SSB IS TRIGGERED DURING THE RECOVERY PERIOD OF THE CAPACITOR, THE OUTPUT PULSE WIDTH WILL BE OF INCORRECT DURATION. THIS CIRCUIT ONLY USES THE 3V SUPPLY AND IS THUS FREE FROM MARGINAL CHECK WHICH THE SSA CIRCUIT HAS.

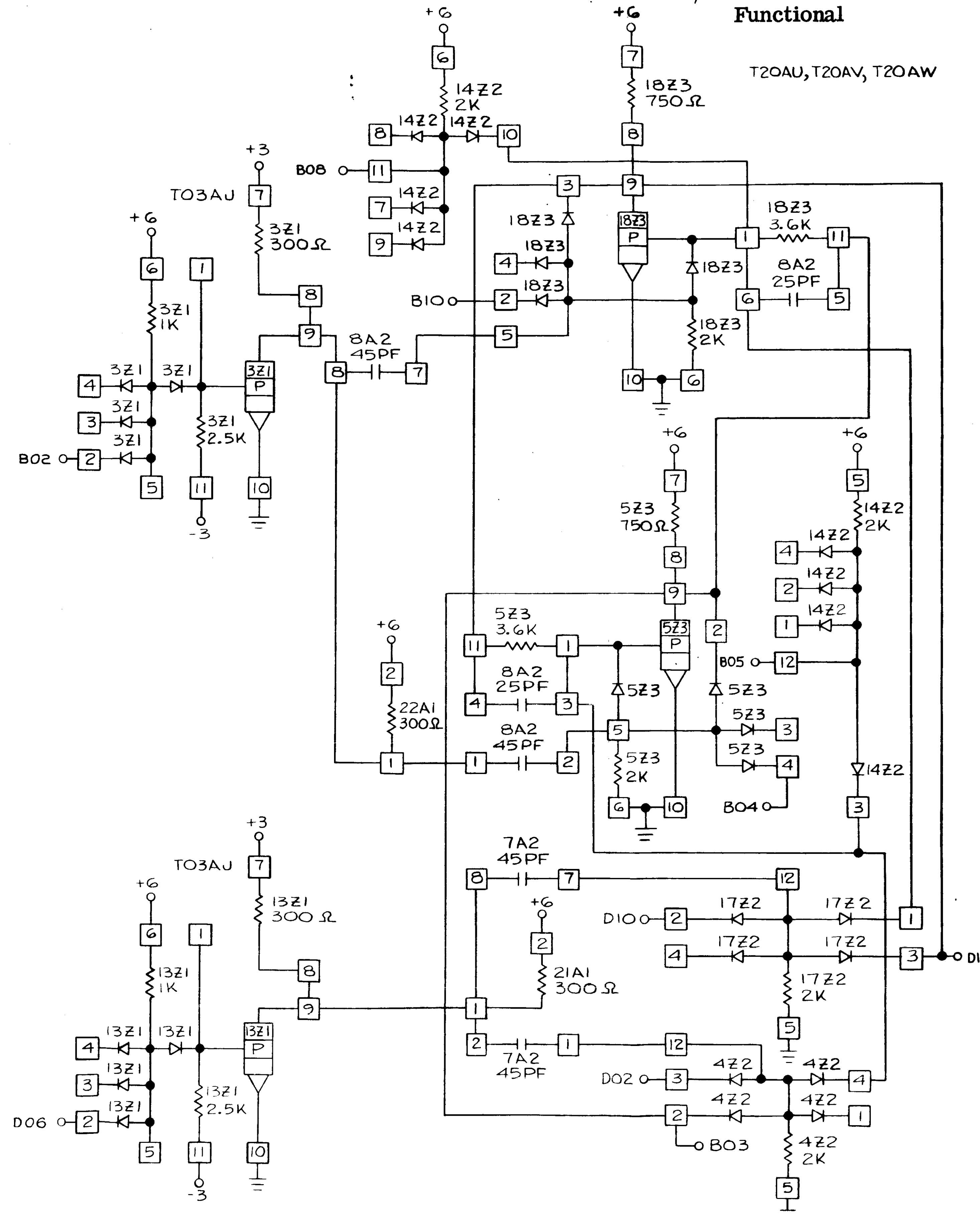


** REF. ONLY-NOT PART OF LOGIC DWG.

2-BINARY AC TRIGGERS P/N 5803683



P/N 5803683
Functional



10 API W/L

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

:

P/N	5803686	
MODULE CODE	MODULE PART NUMBER	QTY
API-3V	361473	10
	2414883	3

CARD TYPE	1-12

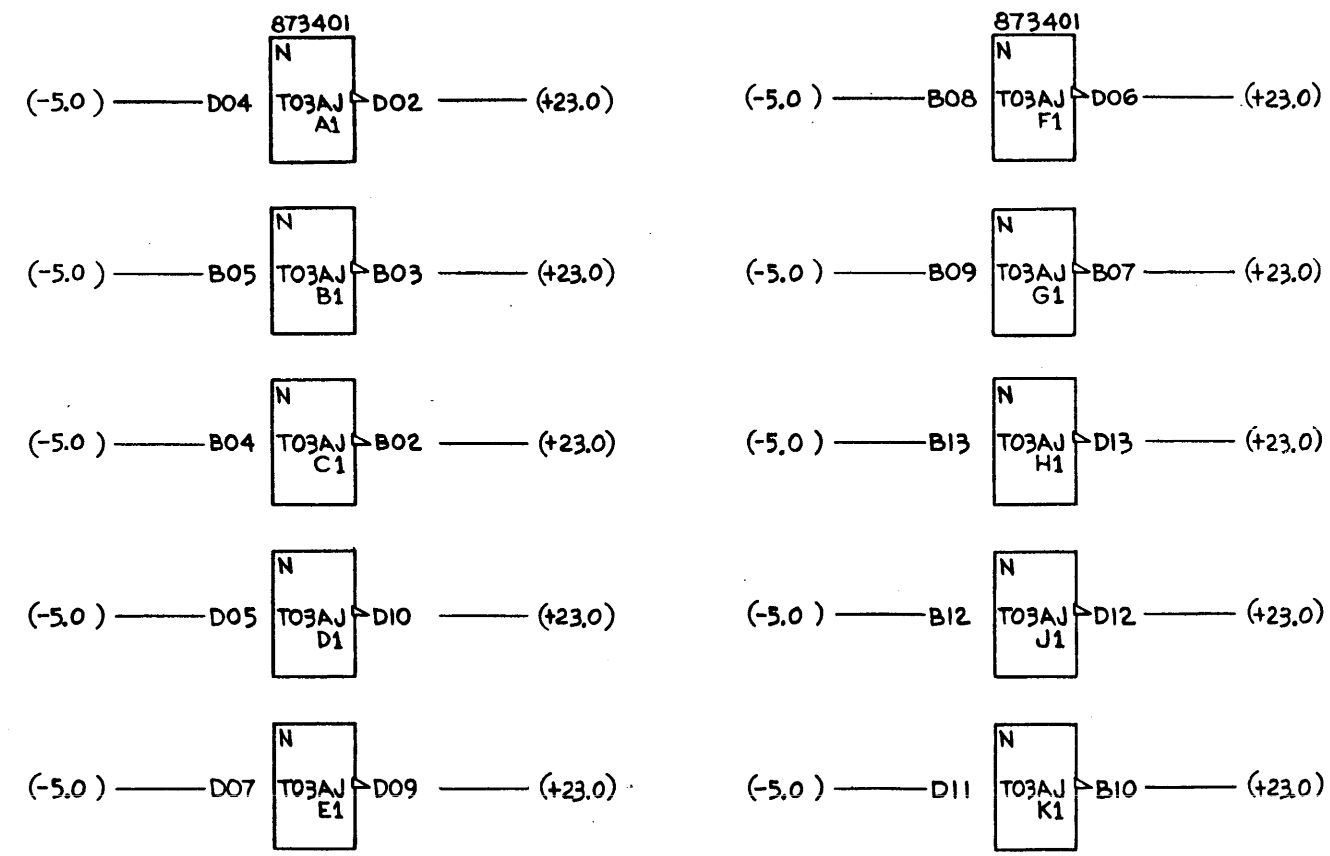


FIGURE 162

3-3WAI HPD W/PL-

PWR REQ

PIN	VOLT
D08	GRD
D07	GRD
D09	GRD
D03	+3
B11	+6
B06	-3

SPECIAL APPLICATION NOTES

P/N	5804061	
MODULE CODE	MODULE PART NUMBER	QTY
HPD	361475	3
AI	361451	3
	2414883	2
	2390445	1

CARD TYPE	1-12

Functional

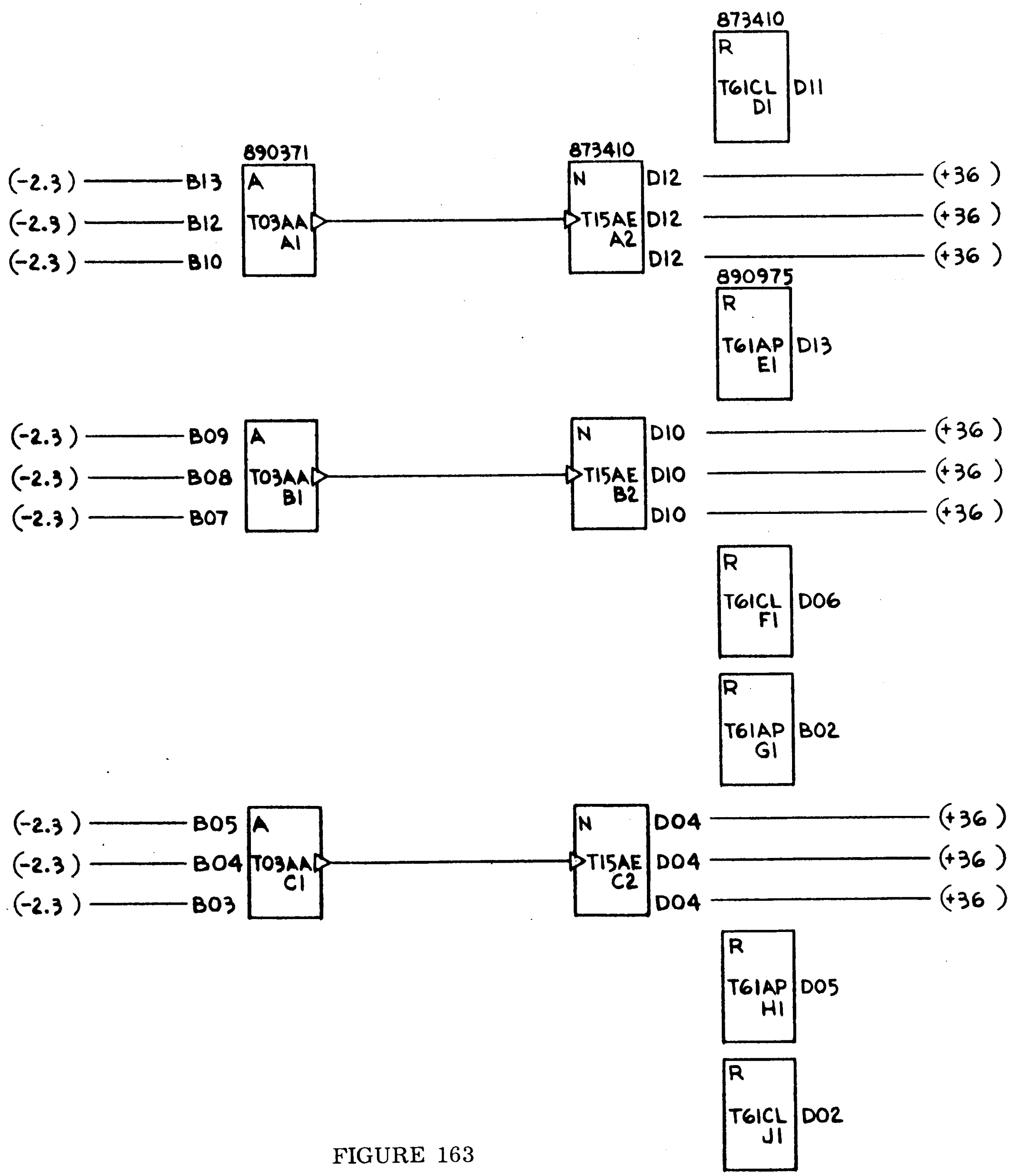


FIGURE 163

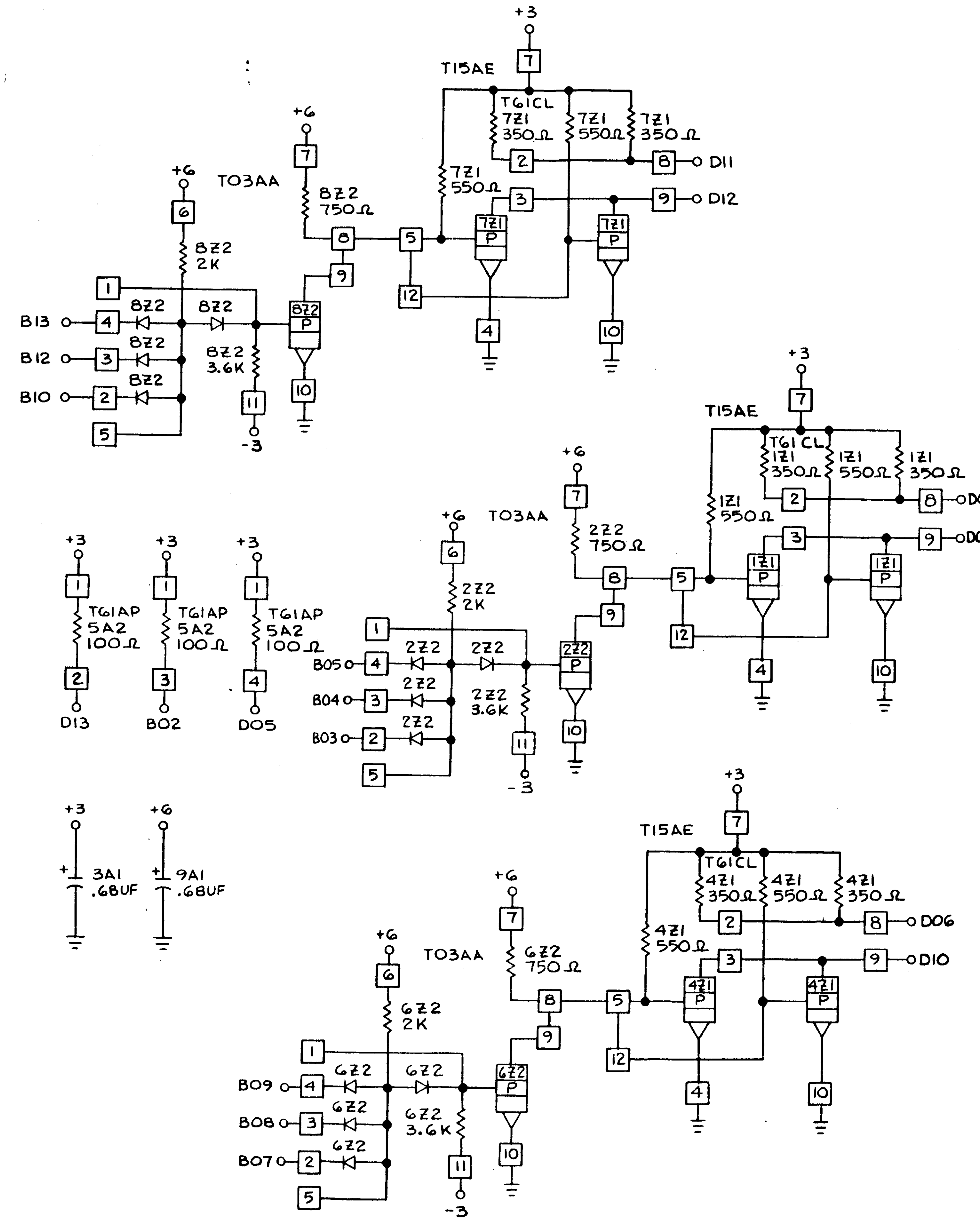

T15AE
T61CL
TO3AA
T61AP
B13
B12
B10
D11
D12
B05
B04
B03
D02
D04
D13
B02
D05
B09
B08
B07
D06
D10
3A1
.68UF
9A1
.68UF

FIGURE 164

9-WAY EXCLUSIVE OR W/L

SPECIAL APPLICATION NOTES

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B06	-3

P/N	5804065	
MODULE CODE	MODULE PART NUMBER	QTY
II	361479	2
AOX	361455	6
AOI	361453	4
	2414883	1

CARD TYPE	1-12

Functional

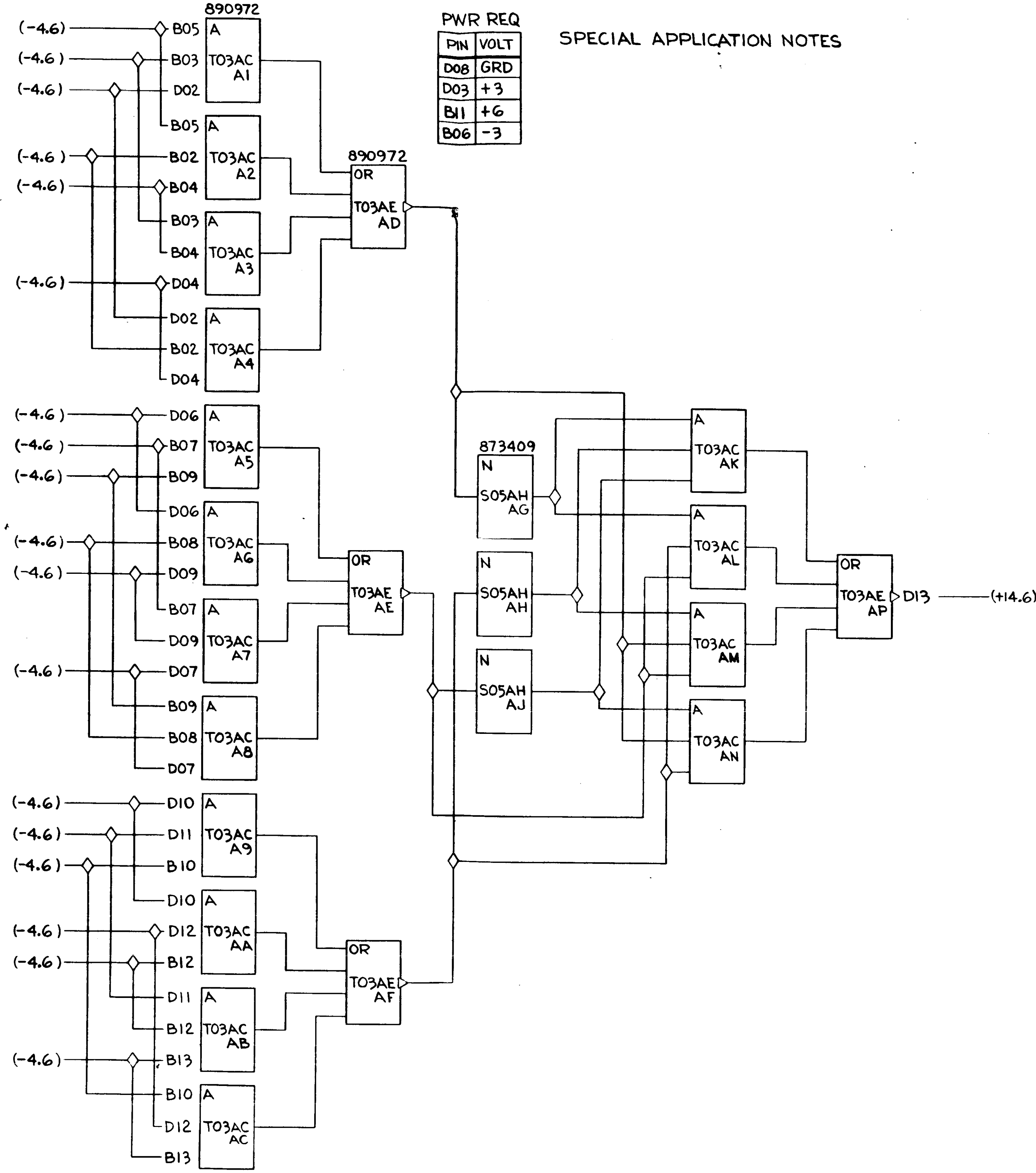


FIGURE 165

9-WAY EXCLUSIVE OR W/L

P/N 5804065

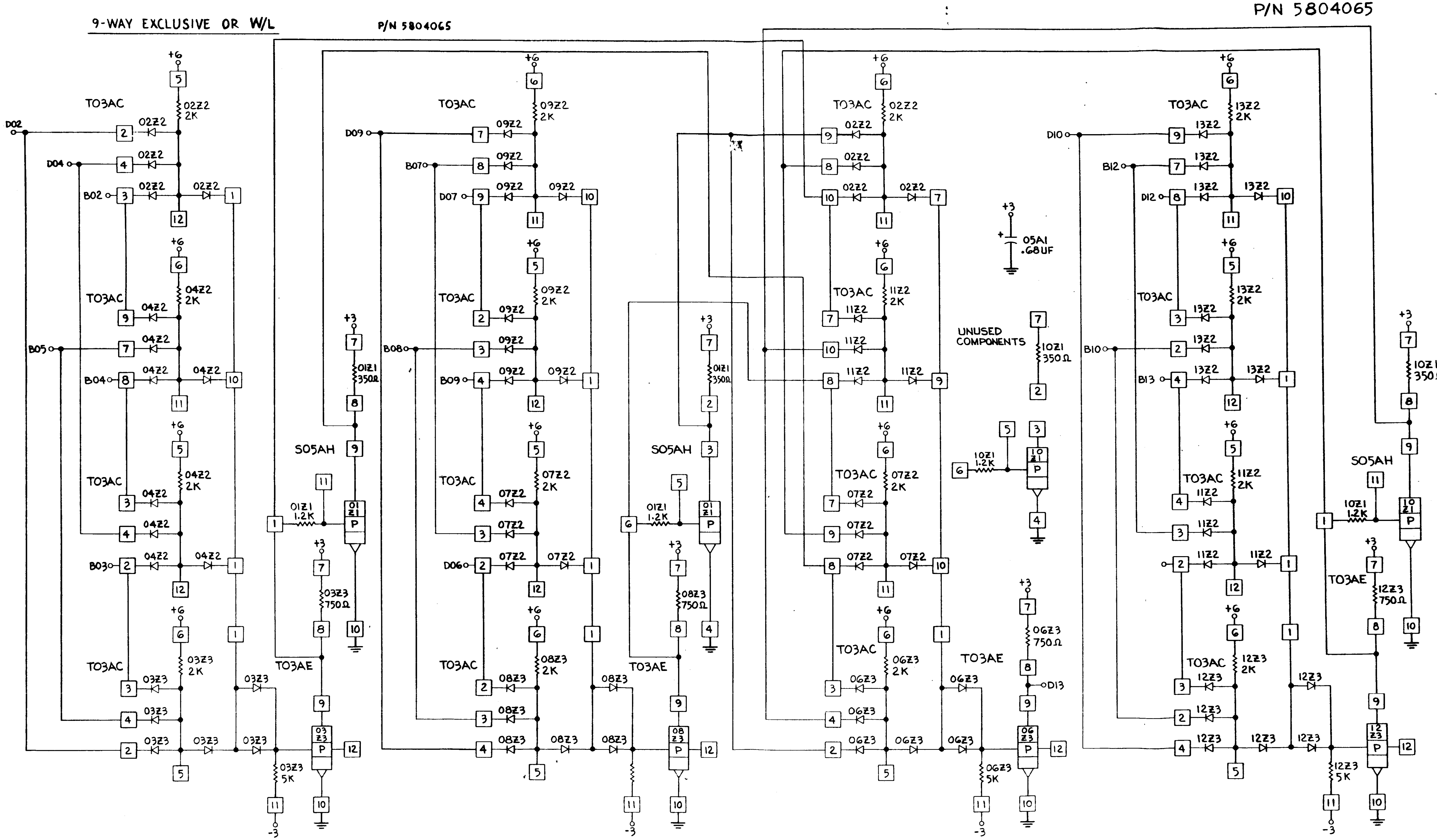


FIGURE 166

10- MULTIPLEX RECEIVERS

PWR REQ

PIN	VOLT
D08	GRD
D03	+3
B11	+6
B6	-3

SPECIAL APPLICATION NOTES
INPUT TO LINE TERMINATORS:
REFER TO TEXT: "LINE DRIVER
AND TERMINATOR RULES"

P/N	5808033	
MODULE CODE	MODULE PART NUMBER	QTY
FTX	361457	5
TX	369183	10
RST	216443	5
RST	216474	2
	2390307	10
	2390308	2
	2390641	1
	2390656	2
RC	2414883	2

CARD TYPE	1-12

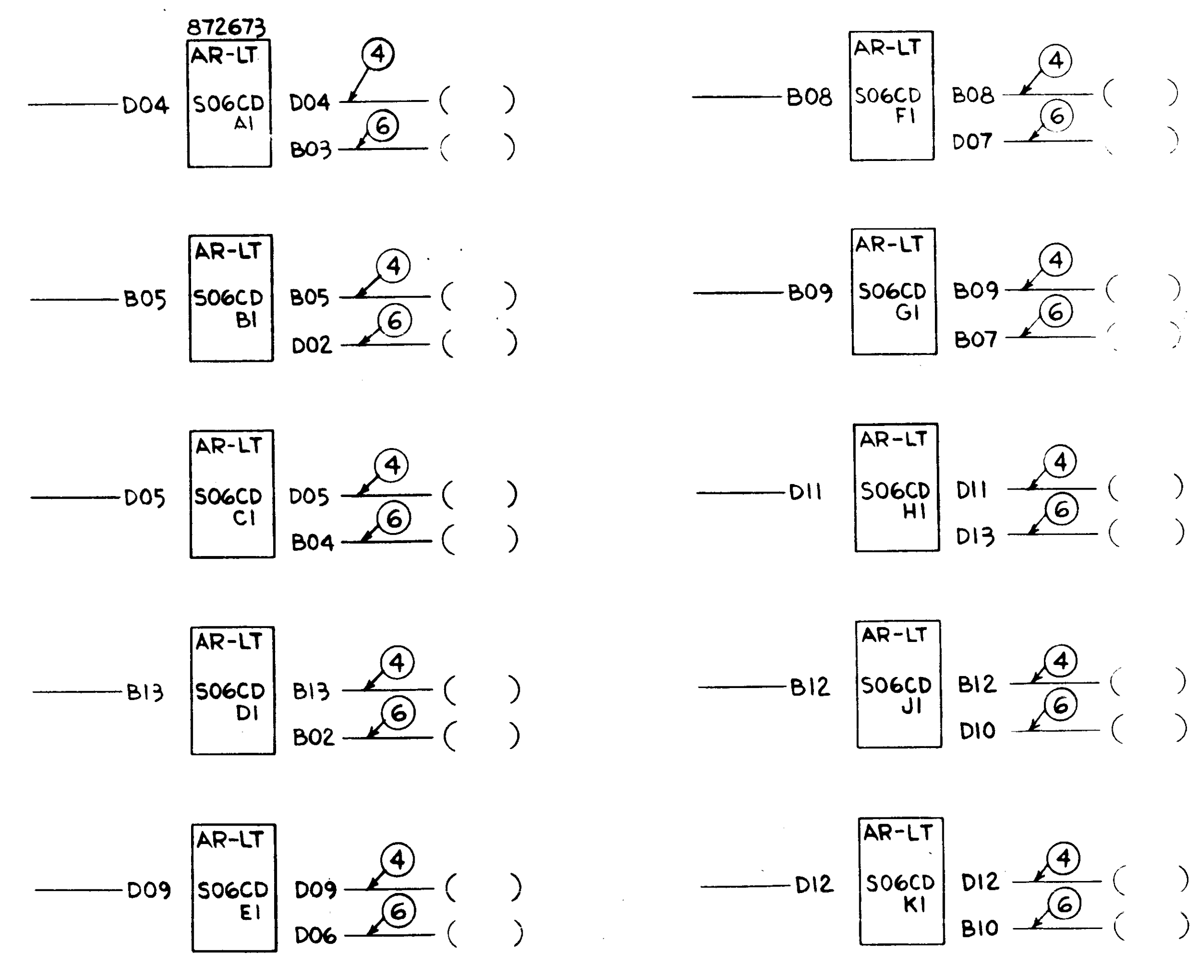


FIGURE 167

6-MULTIPLEX LINE DRIVERS

PWR REQ

PIN	VOLT
B11	+6
D03	+3
B06	-3
D08	GRD
B09	GRD

SPECIAL APPLICATION NOTES:
OUTPUT TO LINE DRIVERS:
REFER TO TEXT "LINE DRIVER AND TERMINATOR RULES"

P/N	5808045	
MODULE CODE	MODULE PART NUMBER	QTY
	216443	6
AOI	361453	6
	2390306	12
	2414818	6
	2414383	3

CARD TYPE	1-12

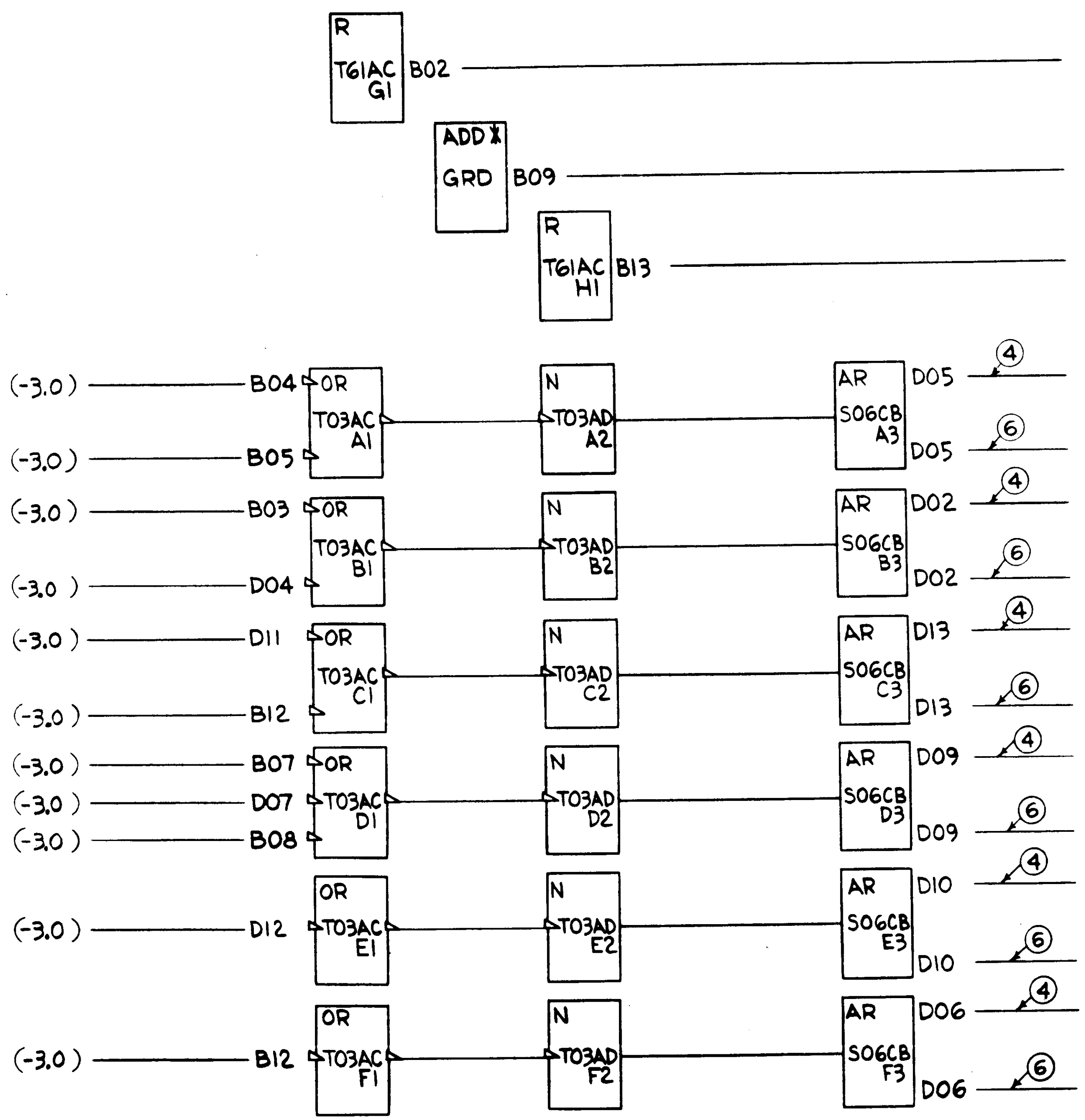


FIGURE 168

BIBLIOGRAPHY

In compiling this manual, information was obtained from the following sources:

1. "Power and Signal Distribution in the SLT Package" (Specification #811800).
2. Field Engineering Manual of Instruction "Solid Logic Technology Component Circuits" Z22-2798-1 (IBM Confidential).
3. CALM List.
4. Circuit Flyer Title and Specification List.